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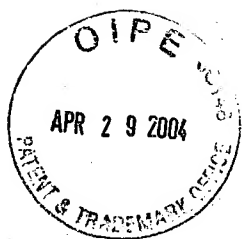
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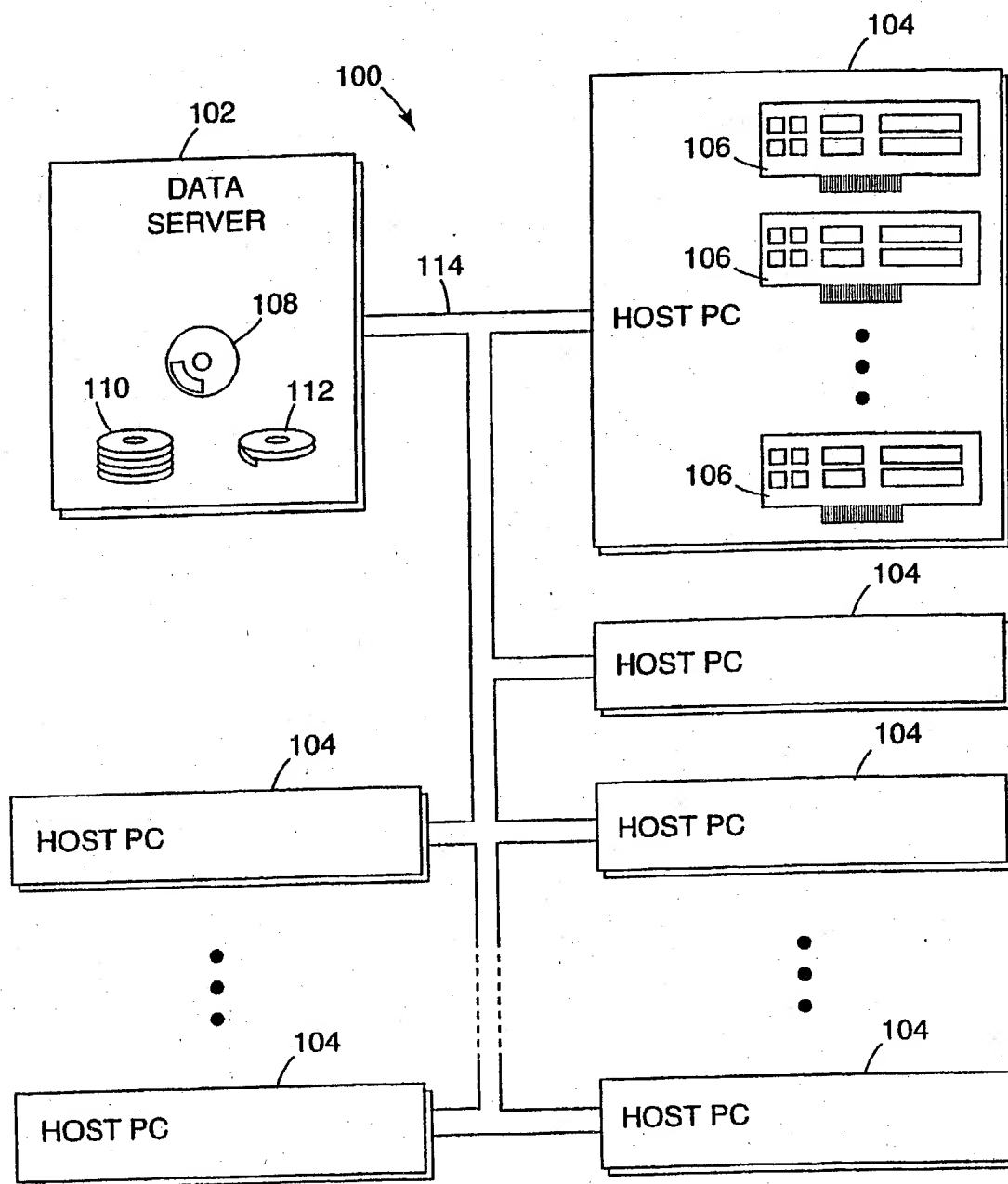


Fig. 1



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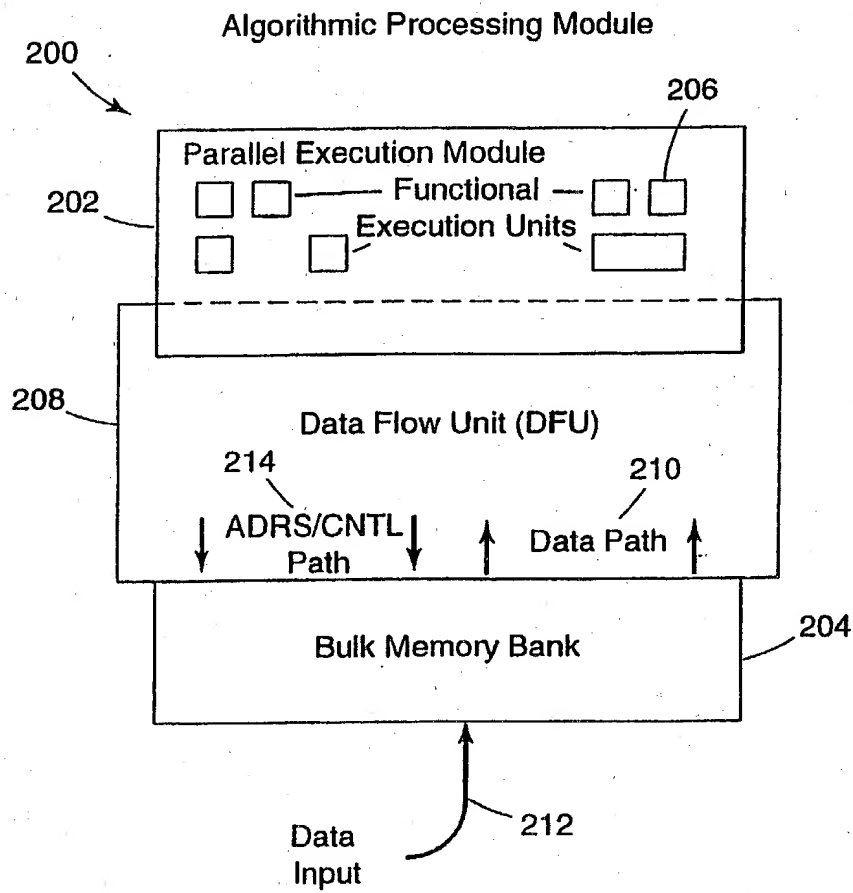


Fig. 2

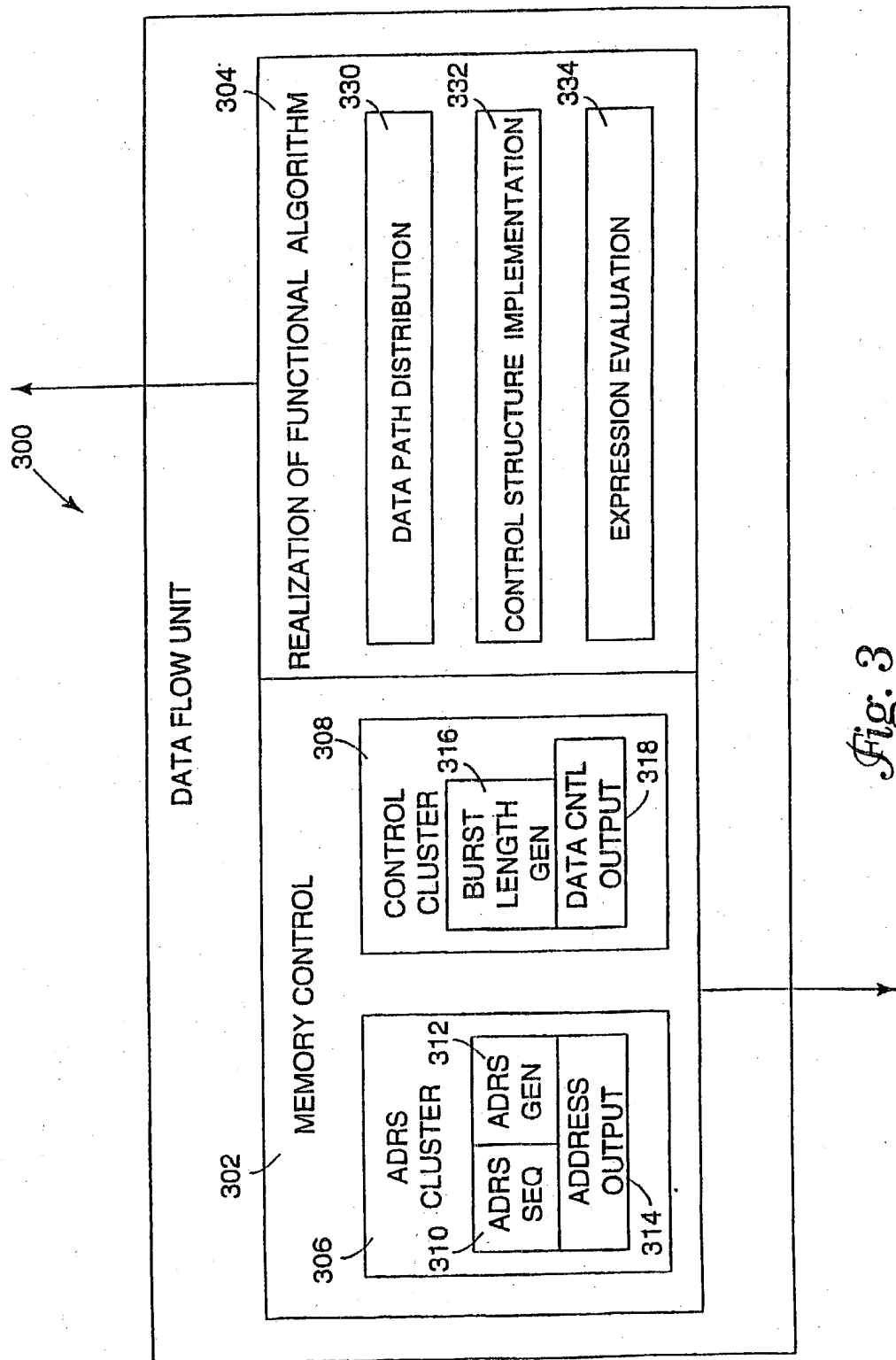


Fig. 3

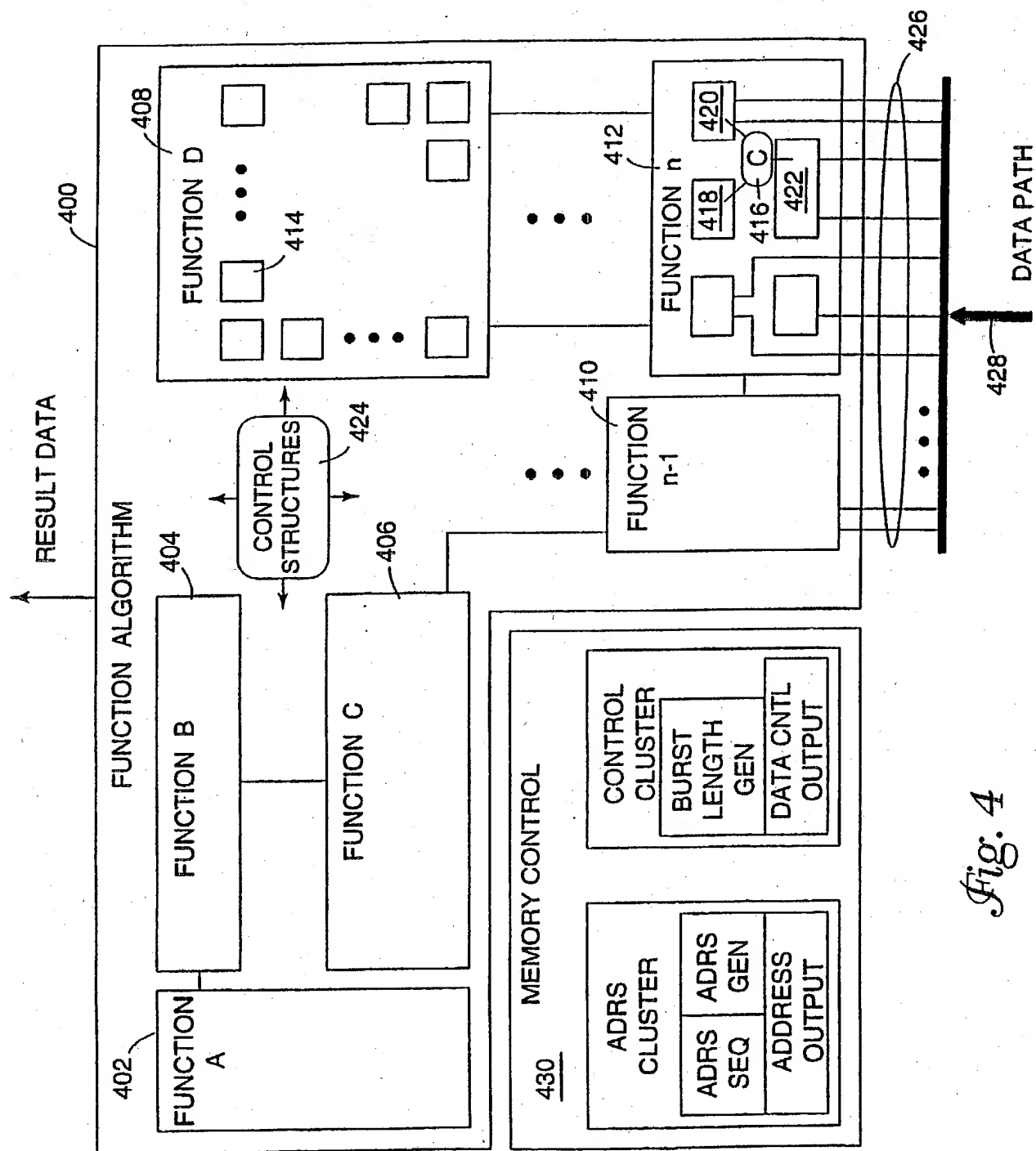


Fig. 4

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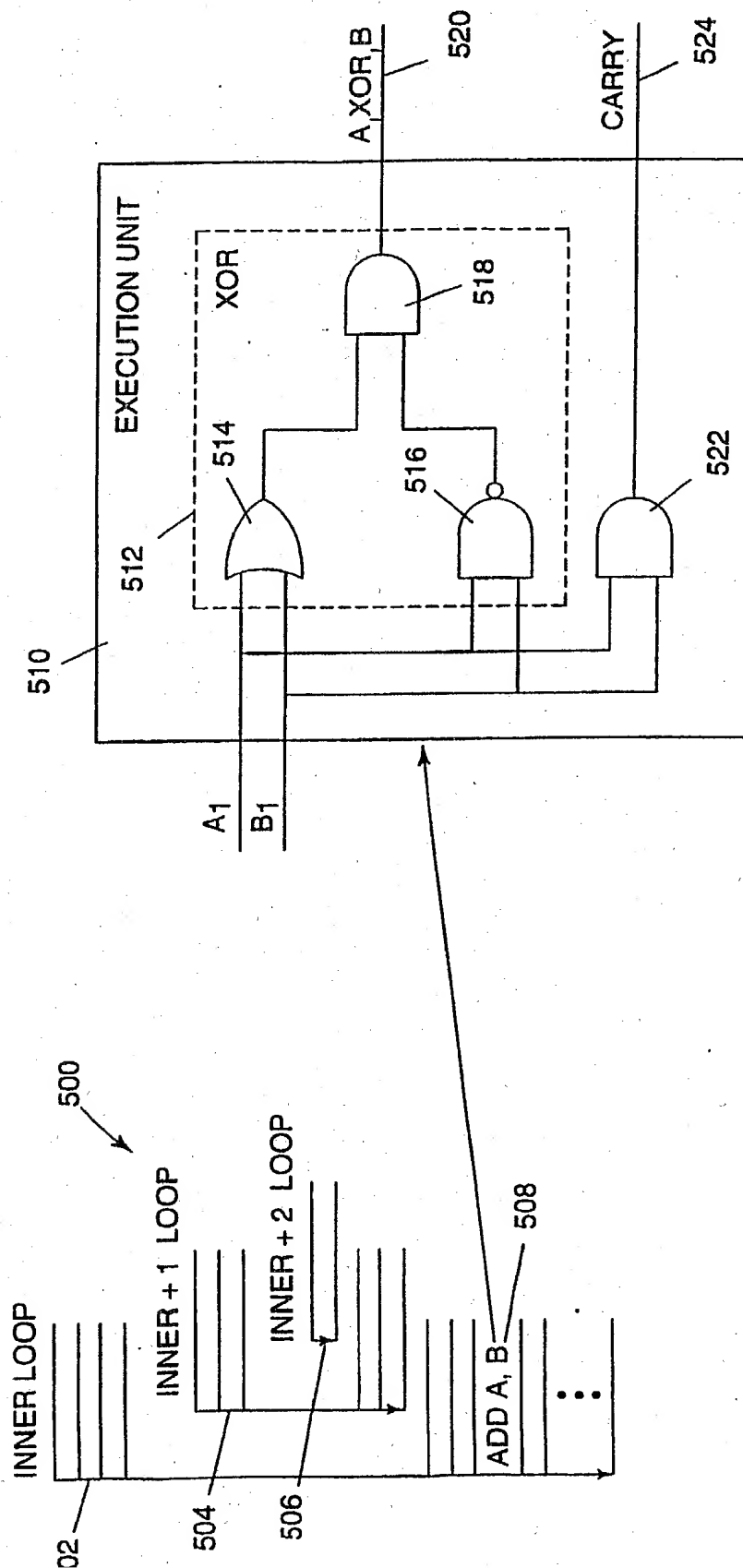


Fig. 5

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Fig. 6A

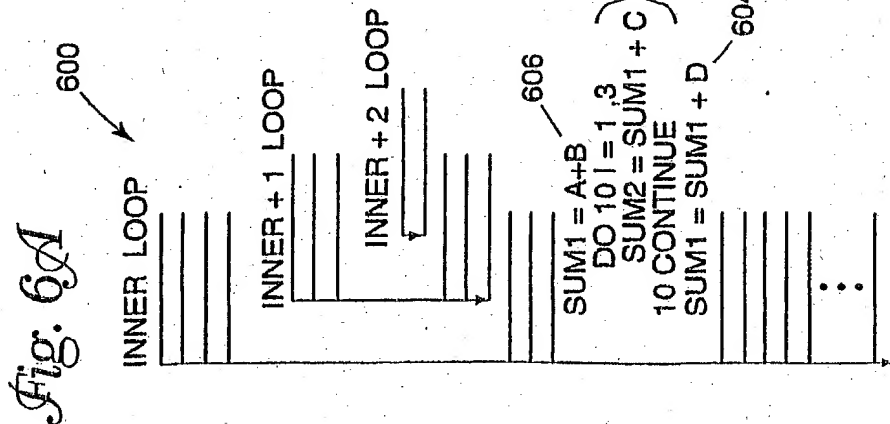


Fig. 6B

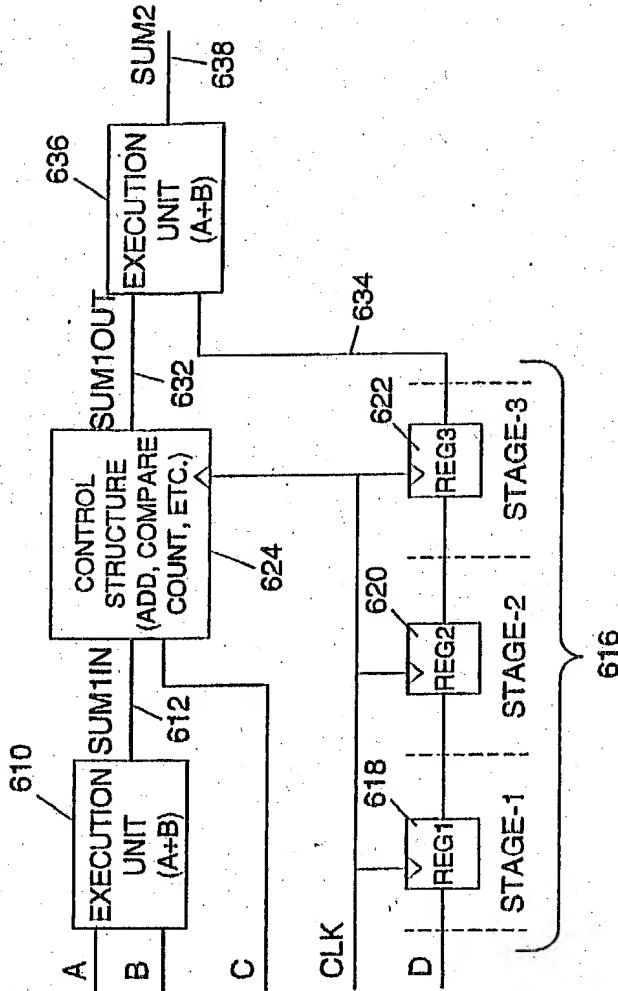
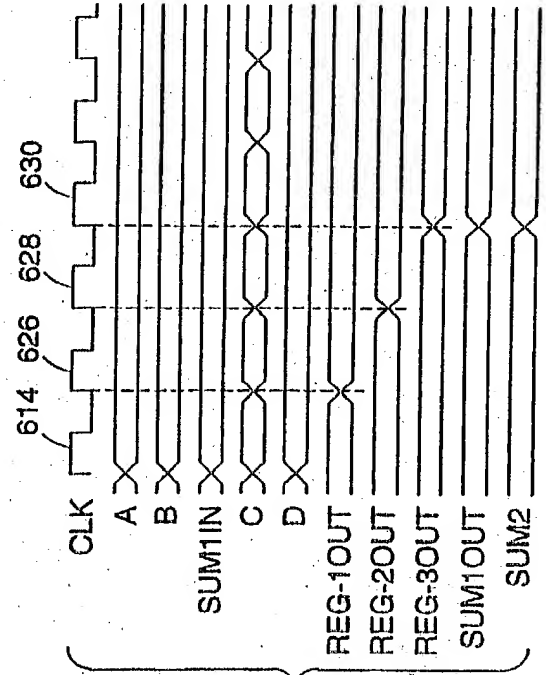
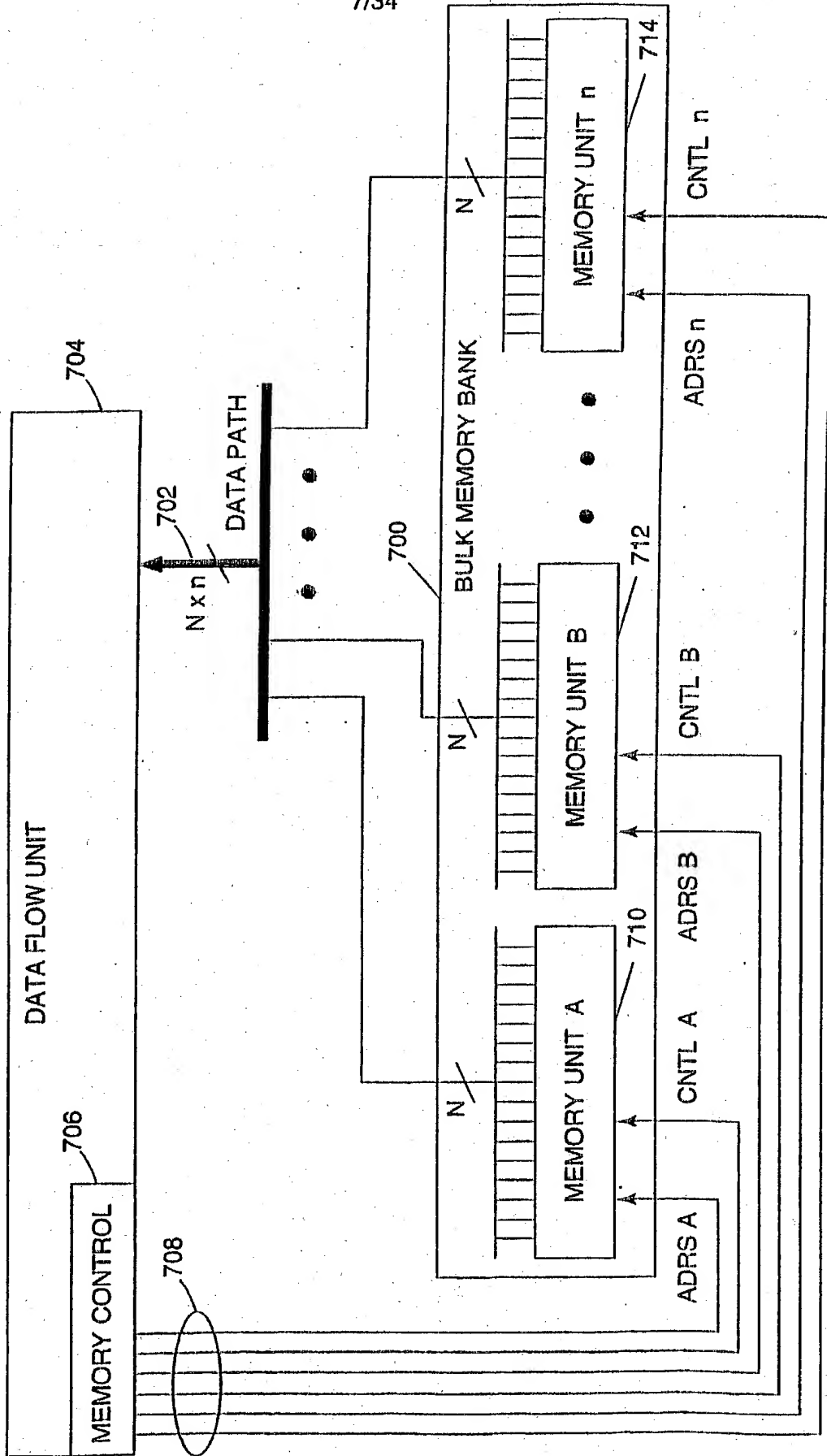


Fig. 6C



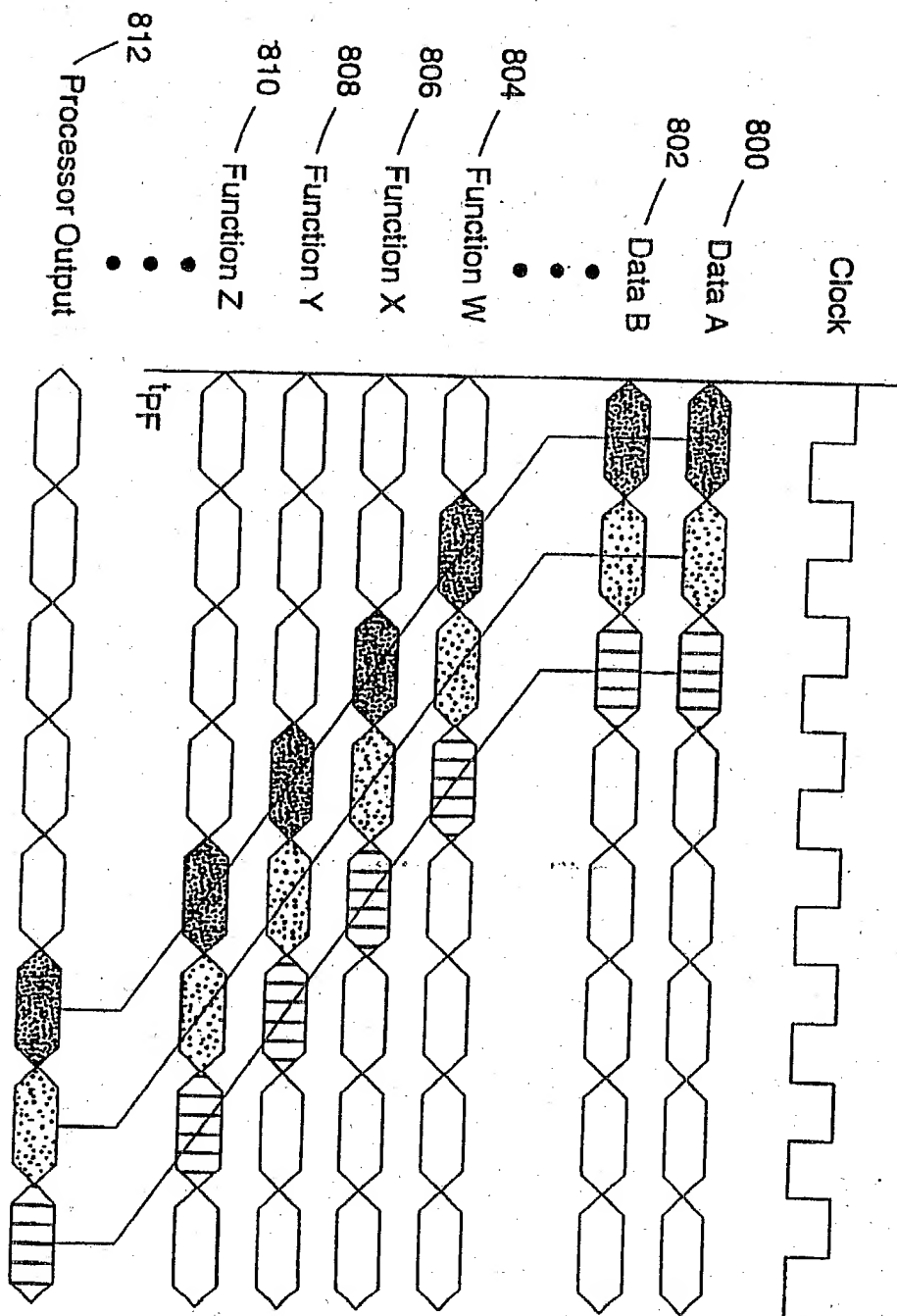
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Fig. 7



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Fig. 8



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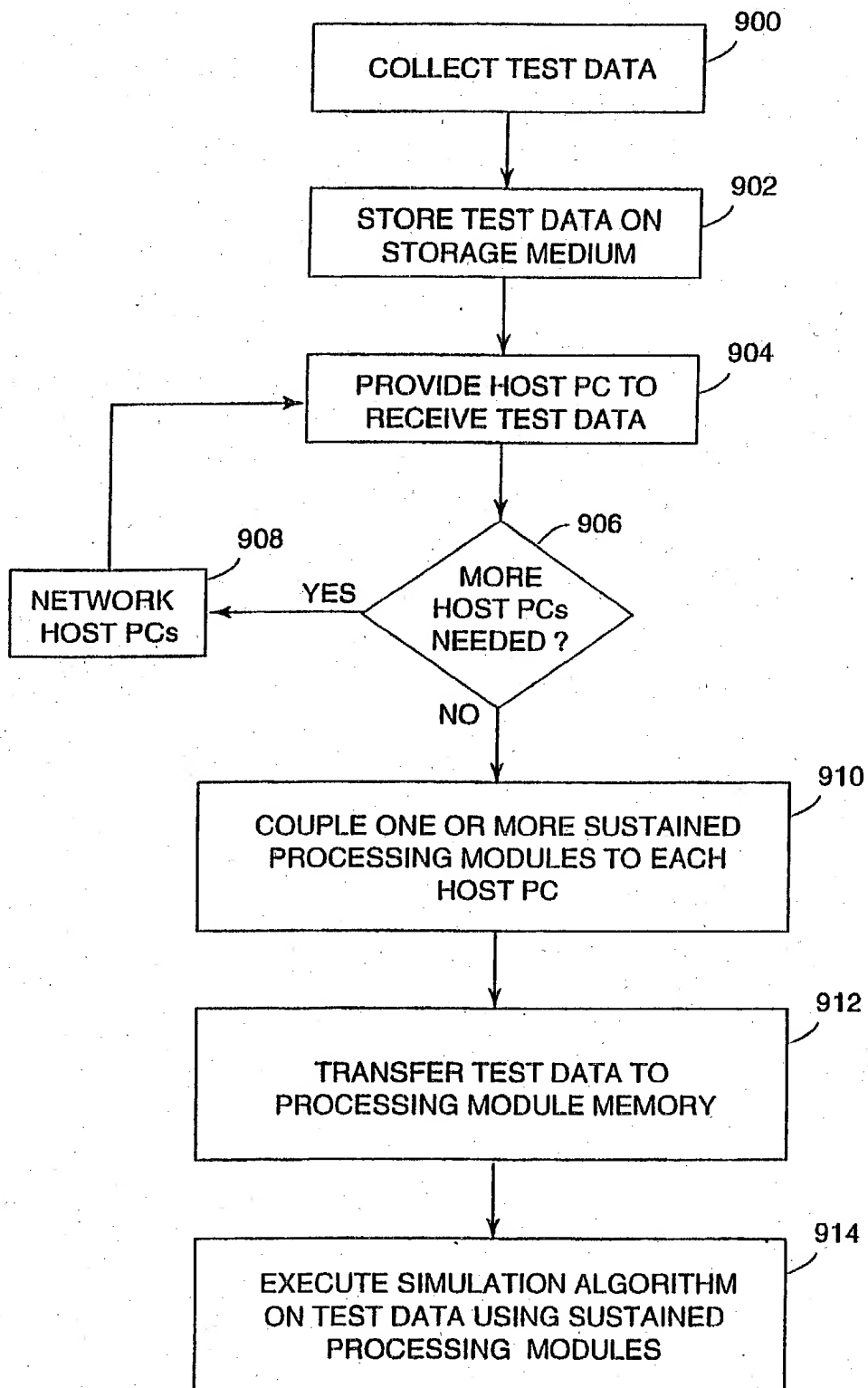


Fig. 9

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SUBROUTINE AVERAGE (INDATA, COUNT, MAX, MIN, AVG, RMS)

INTEGER COUNT

REAL INDATA (COUNT), MAX, MIN, AVG, RMS

1000

C
C These are the inputs and outputs to the function
C name type mode length description
C =====
C
C INDATA R In COUNT Array of input values
C COUNT I In Number of values to average
C MAX R InOut Maximum value found
C MIN R InOut Minimum value found
C AVG R Out Average of all values
C RMS R Out Root-Mean-Square of all values
C

REAL SUM, RMSSUM

INTEGER I

1002

C These are internal variables

C Initialization of internal variables

SUM = 0.0

RMSSUM = 0.0

1004

C Main Loop proper

DO 100 = 1, COUNT

IF (INDATA (I) .LT. MIN) THEN

MIN = INDATA (I)

ENDIF

IF (INDATA (I) .GT. MAX) THEN

MAX = INDATA (I)

ENDIF

SUM = SUM + INDATA (I)

RMSSUM = RMSSUM + INDATA (I) * INDATA (I)

100 CONTINUE

C End of main loop

C Calculate average, RMS

AVG = SUM / COUNT

RMSSUM = SQRT (RMSSUM / COUNT)

END

1016

1018

Fig. 10

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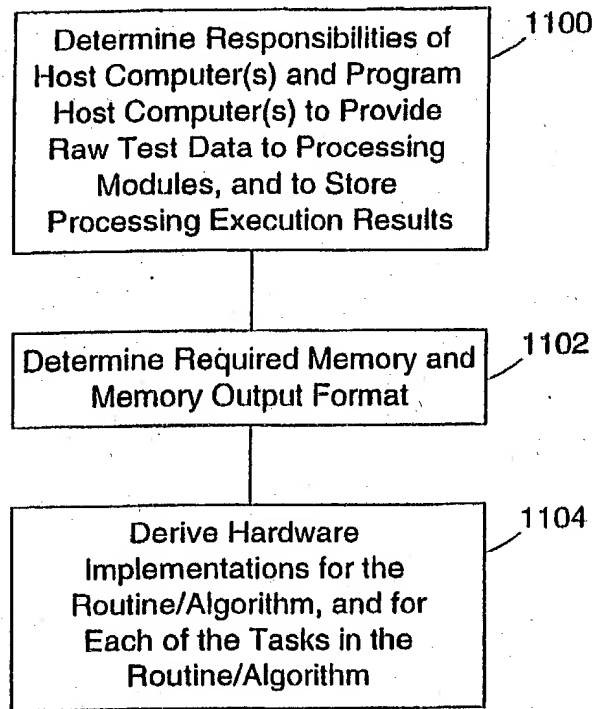
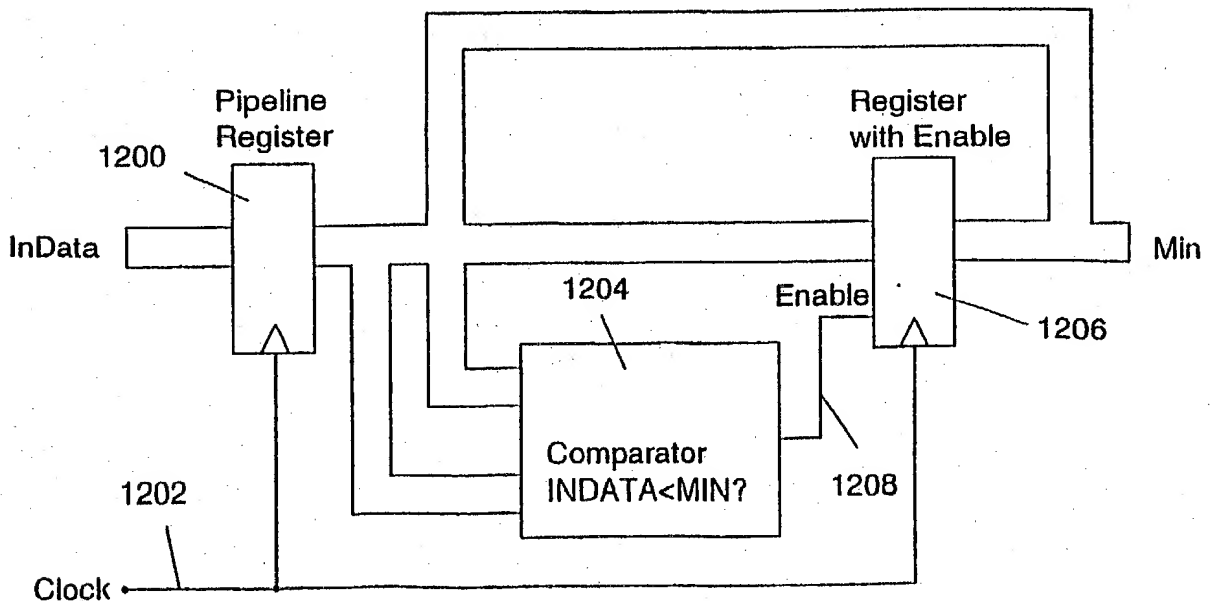


Fig. 11

Fig. 12

```

IF (INDATA (I) .LT. MIN) THEN
  MIN = INDATA (I)
ENDIF
  
```



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Fig. 13

IF (INDATA (I) .LT. MIN) THEN
MIN = INDATA (I)
ENDIF

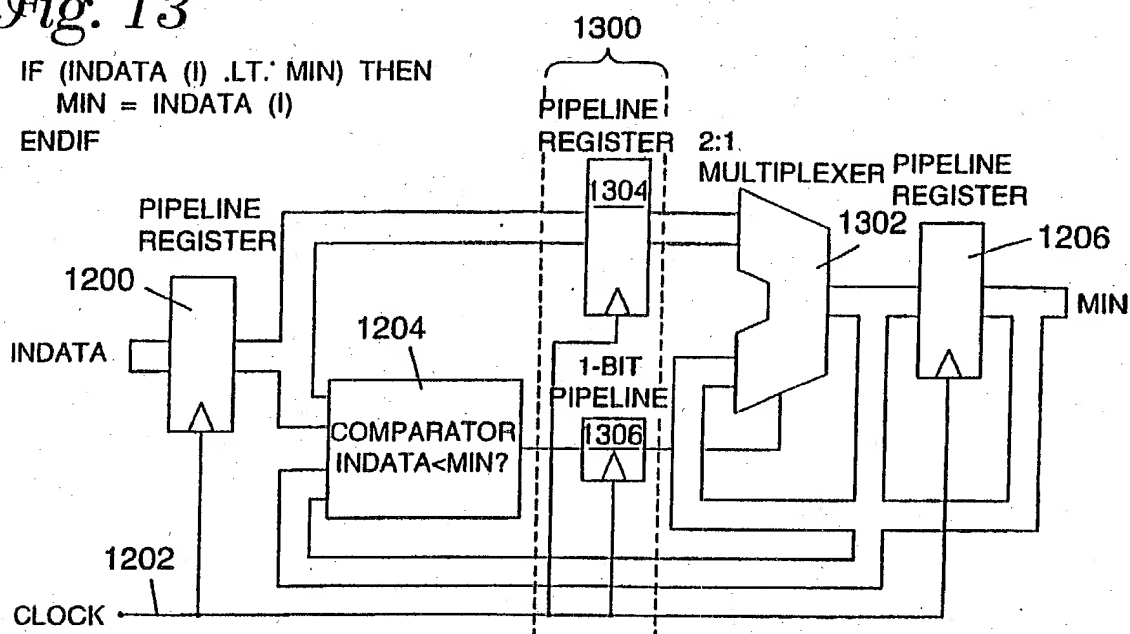
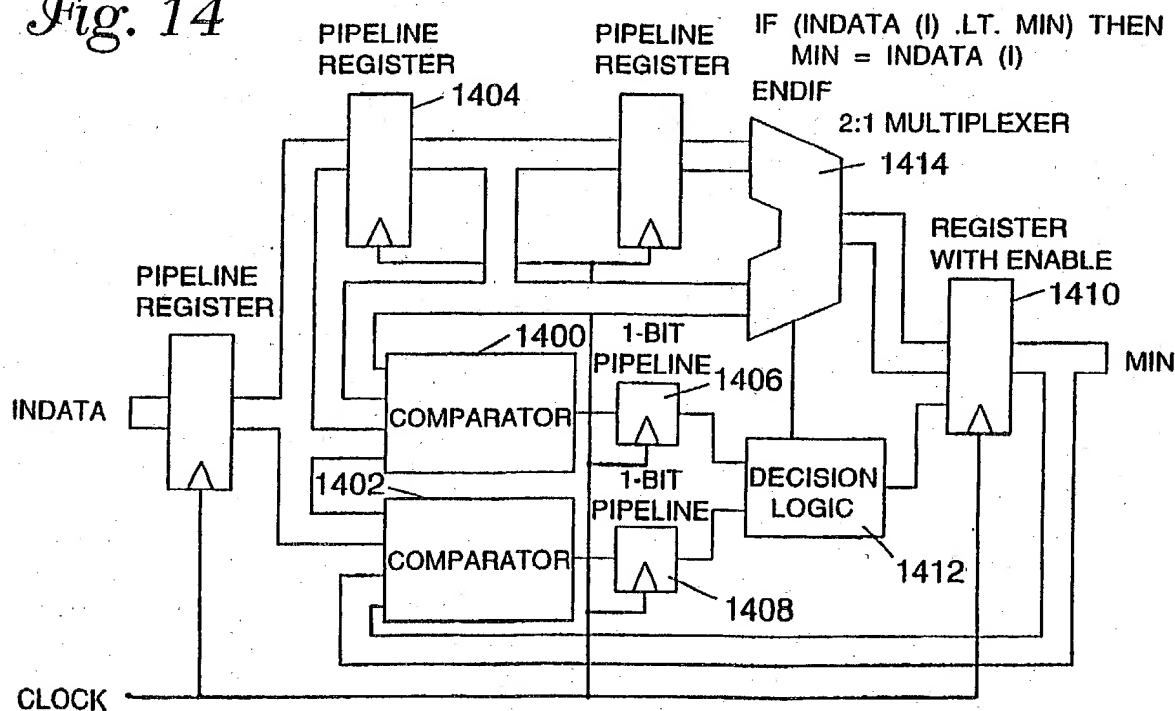


Fig. 14



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Fig. 15

$$\text{SUM} = \text{SUM} + \text{INDATA (I)}$$

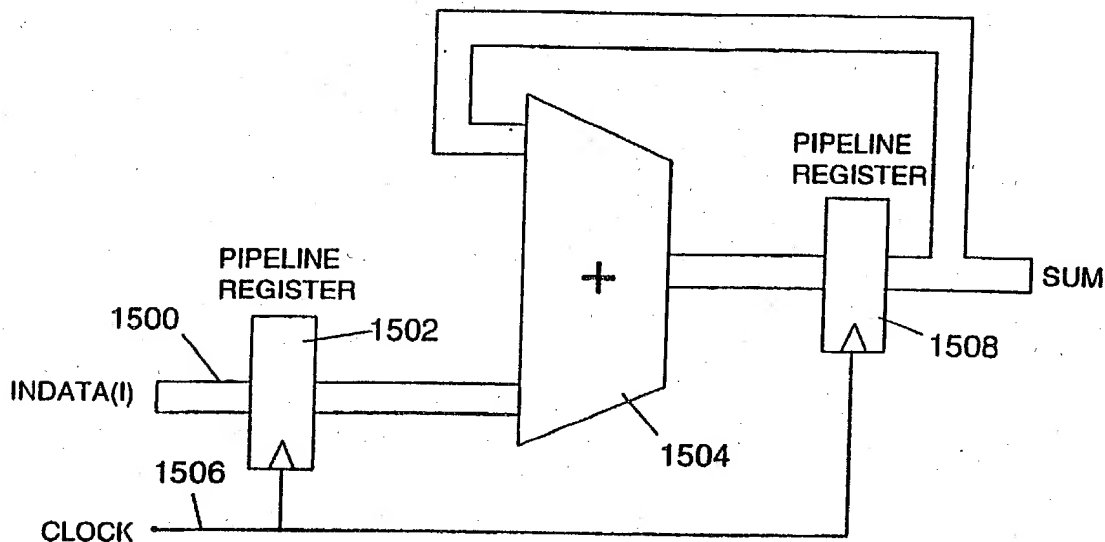
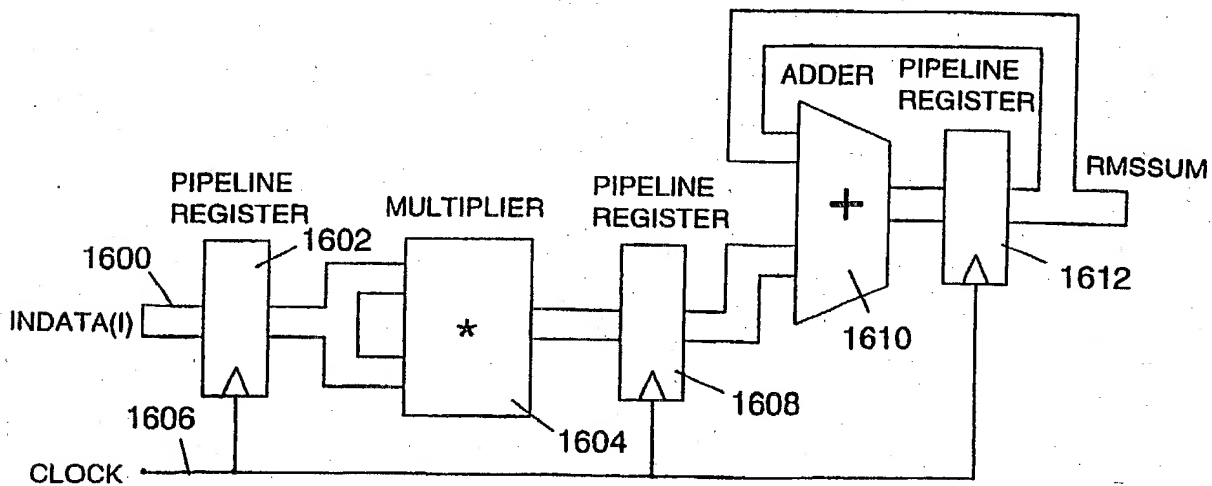


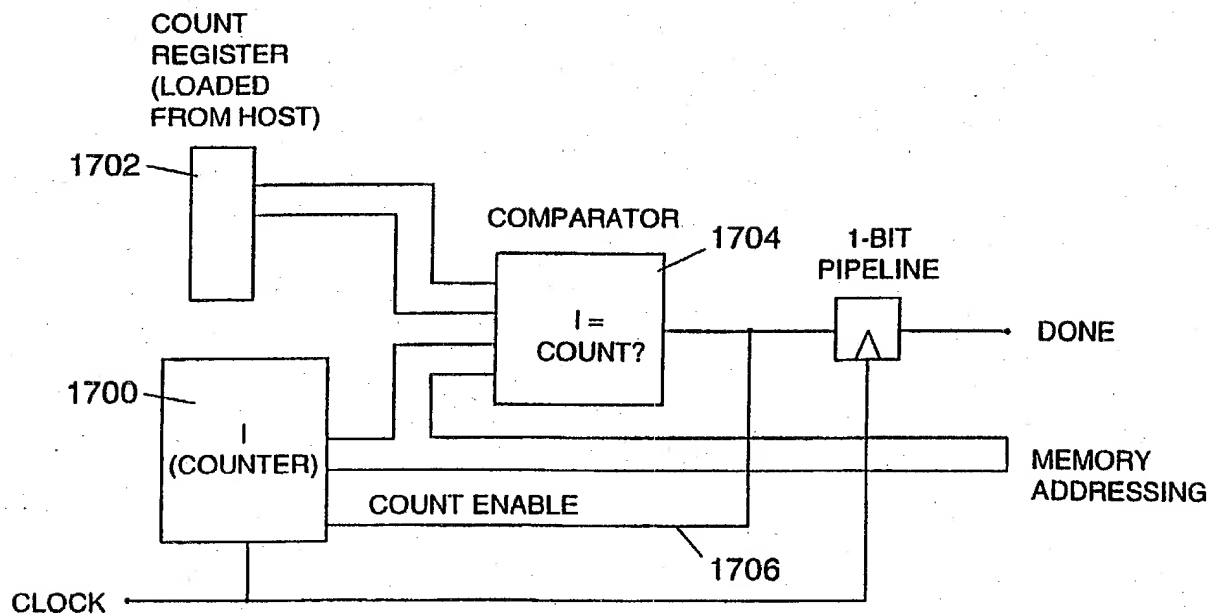
Fig. 16

$$\text{RMSSUM} = \text{RMSSUM} + \text{INDATA (I)} * \text{INDATA (I)}$$



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Fig. 17



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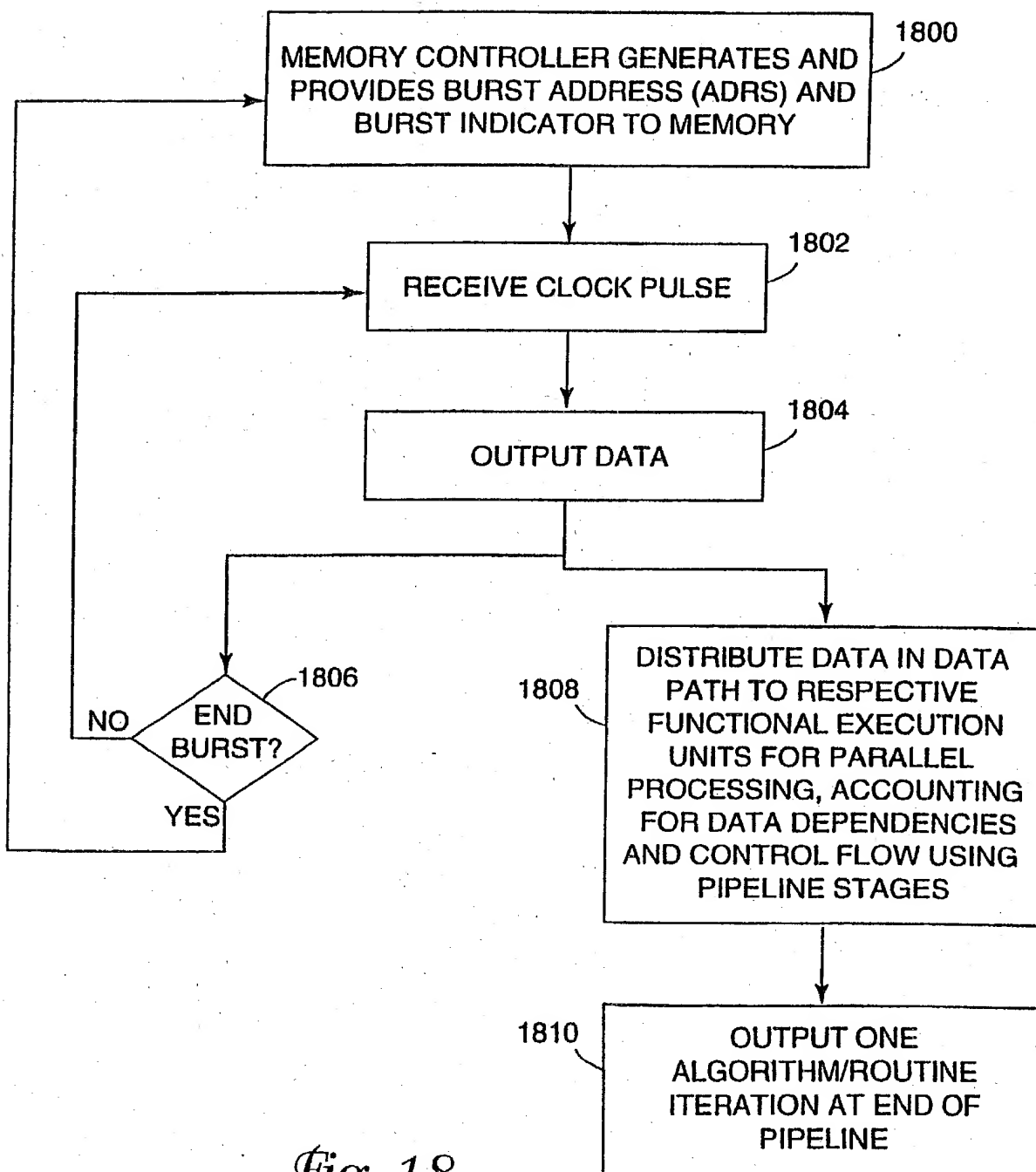
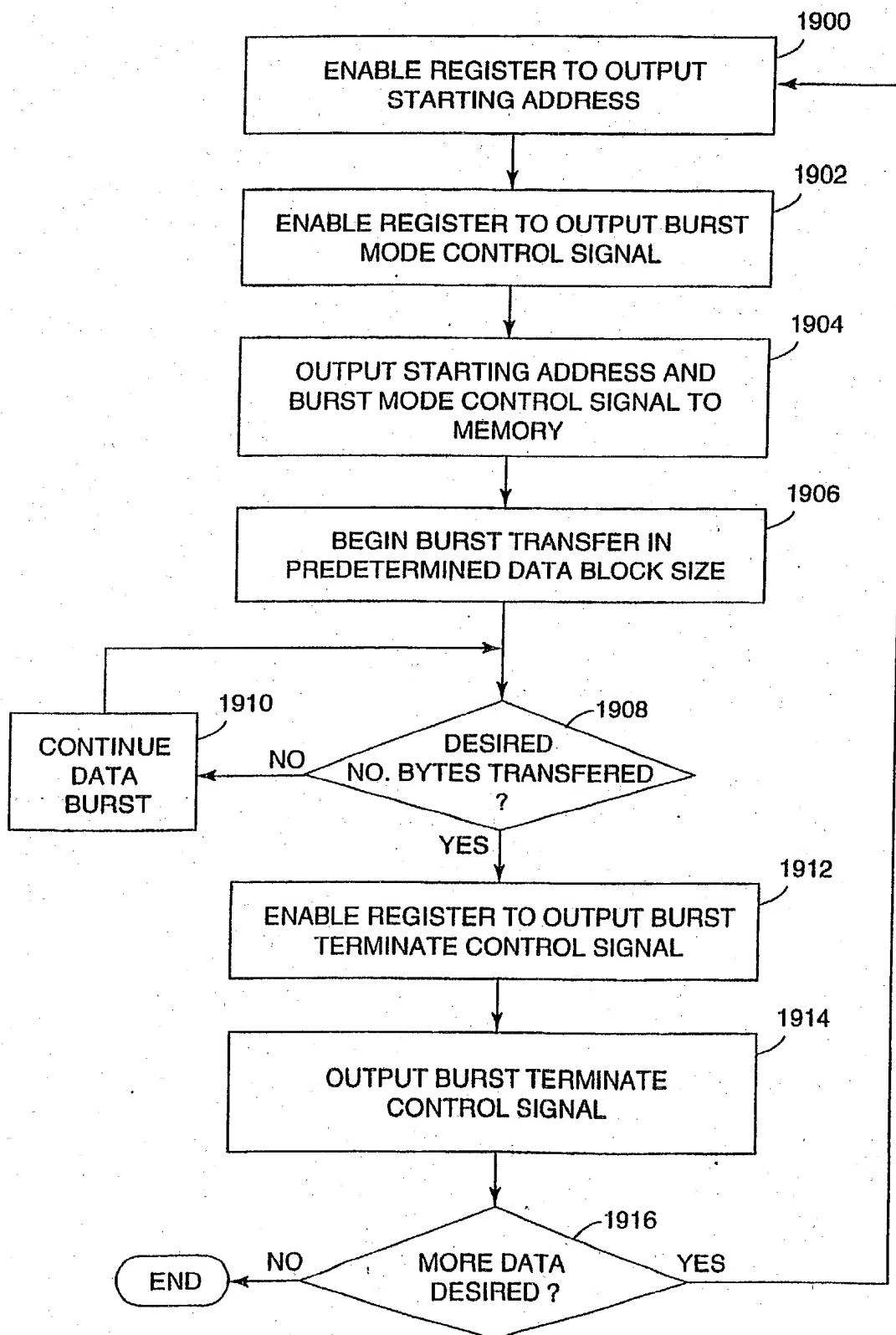


Fig. 18



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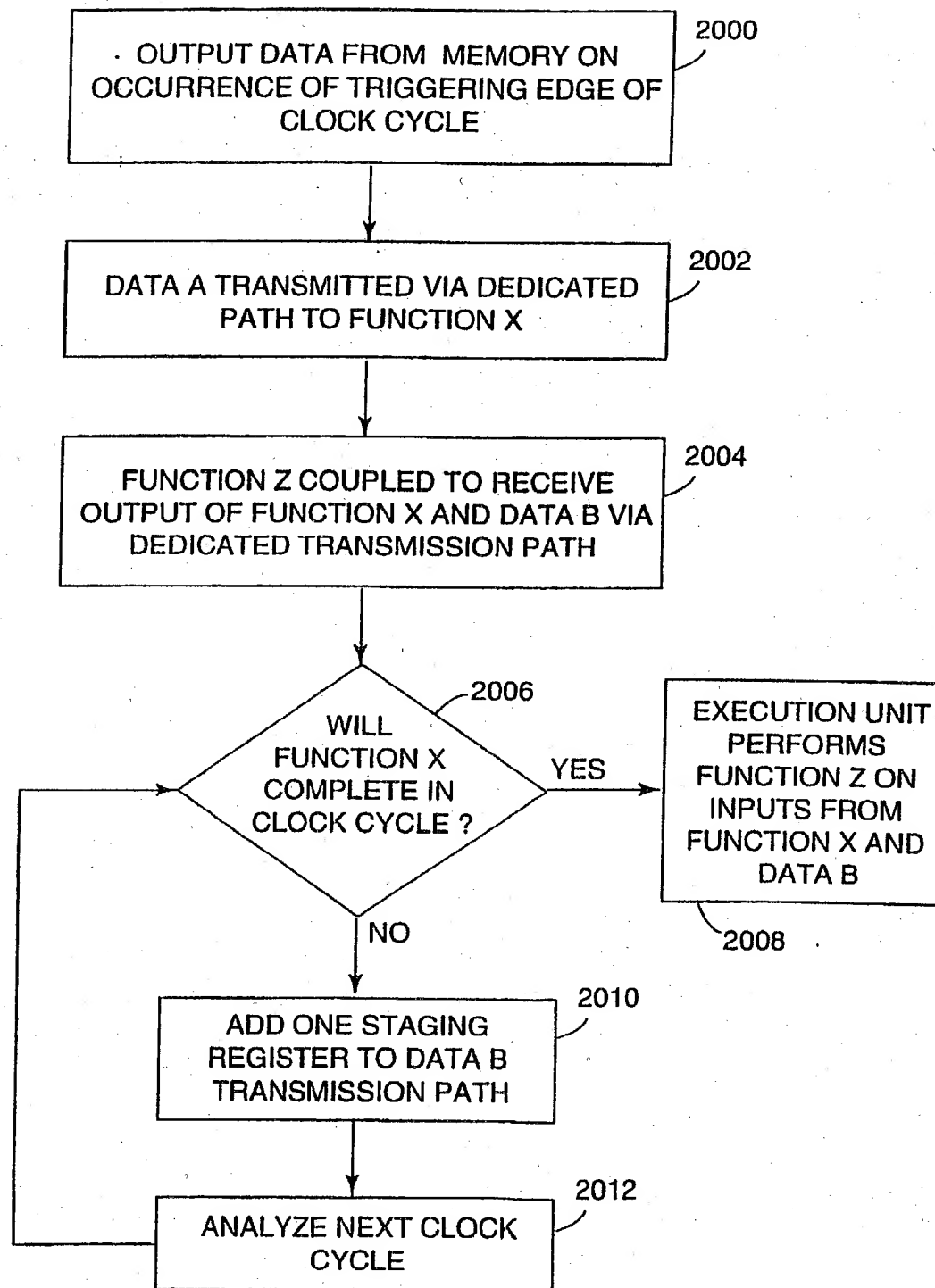
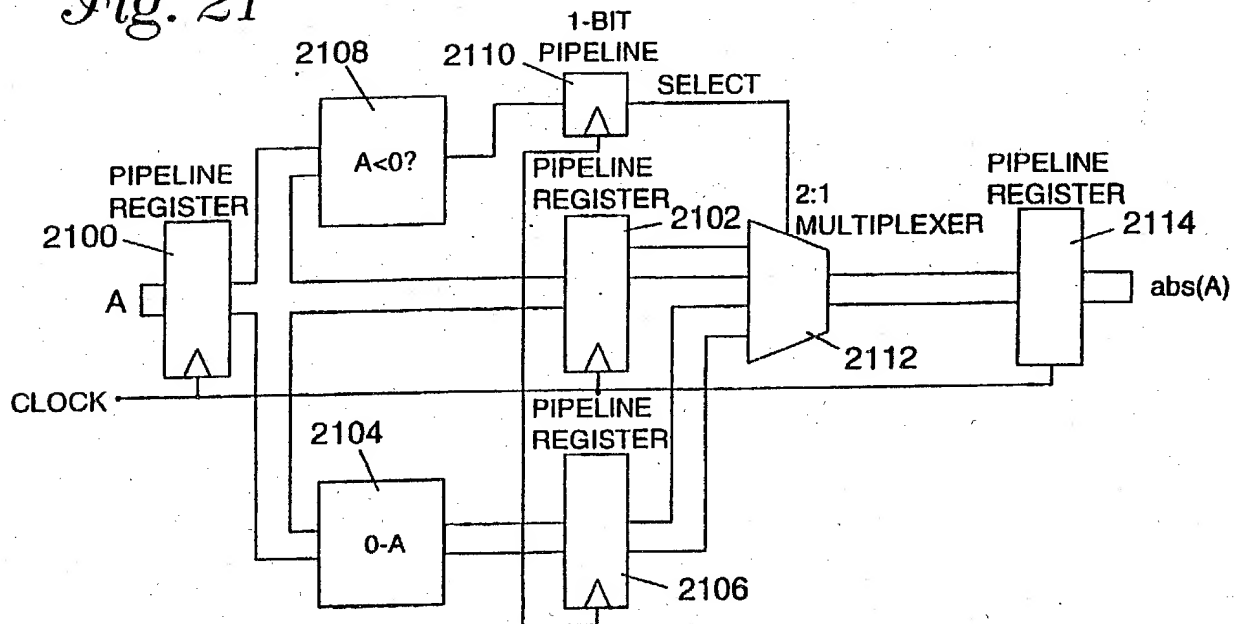


Fig. 20

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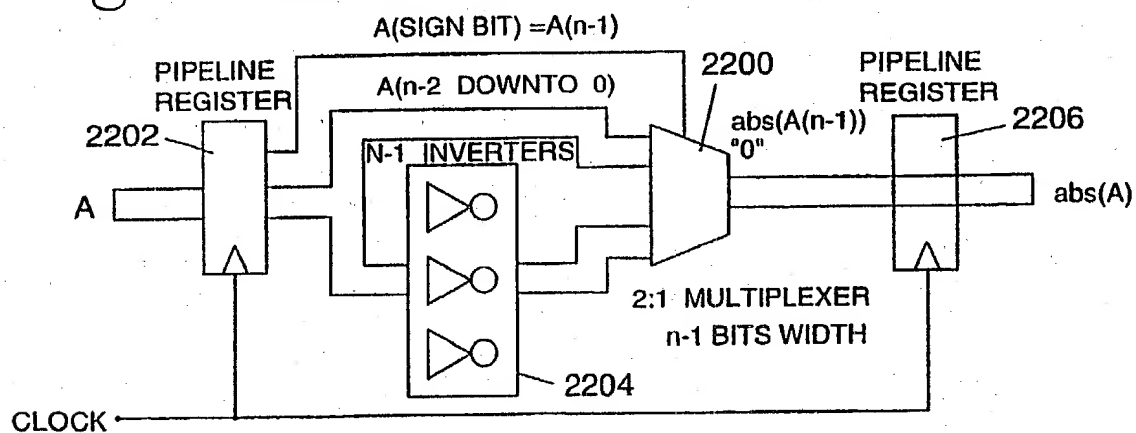
Fig. 21



abs(a) NAIVE HARDWARE IMPLEMENTATION - 2 CYCLES

Fig. 22

Note:- A width = N bits



abs(a) FASTER IMPLEMENTATION - 1 CYCLE

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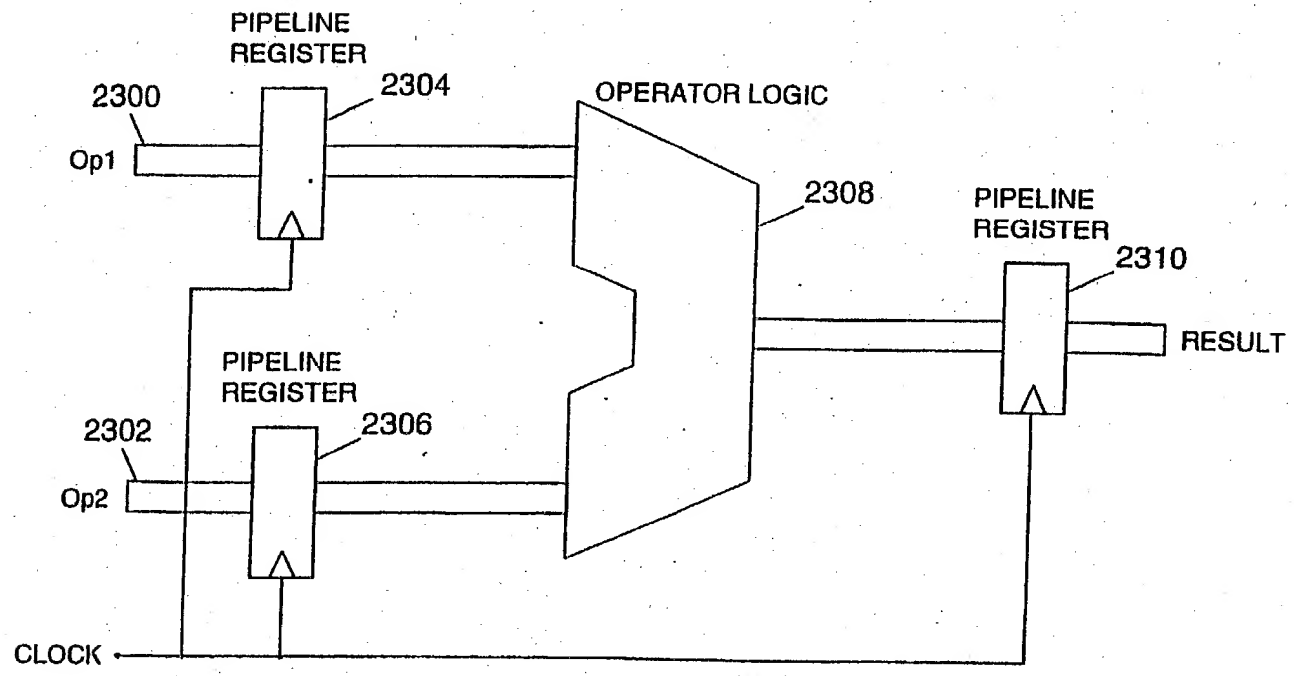


Fig. 23 BINARY OPERATOR

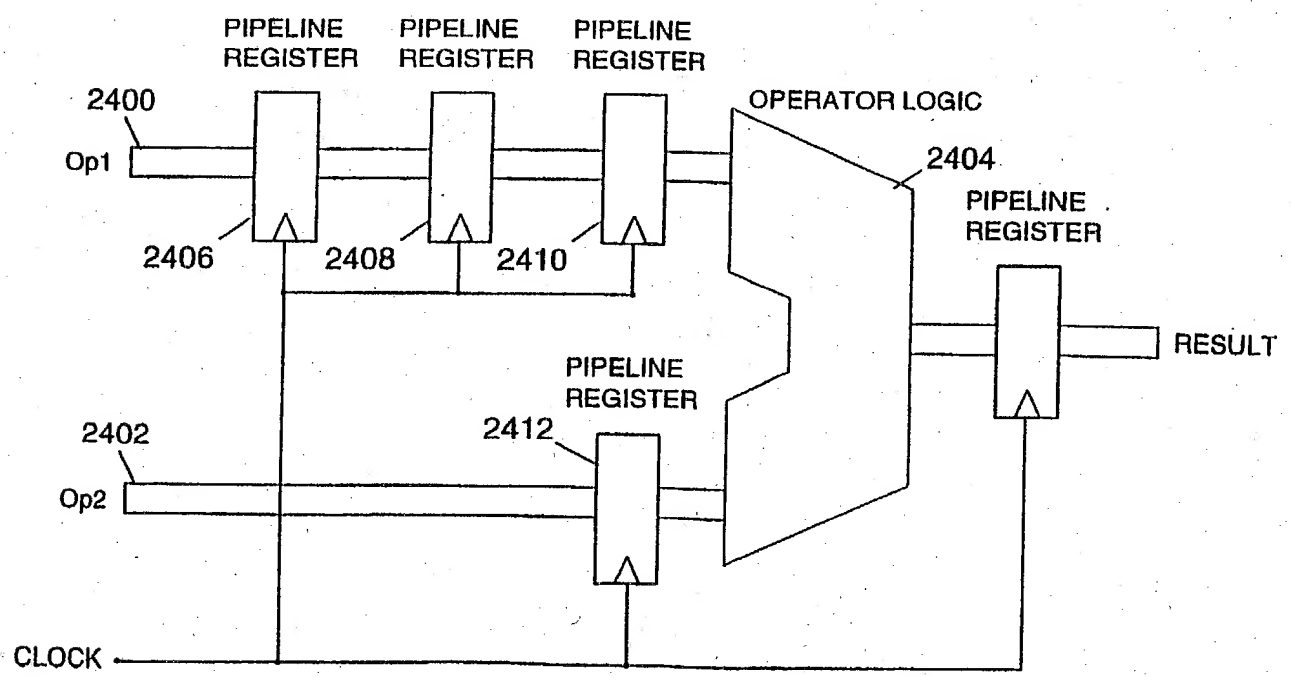
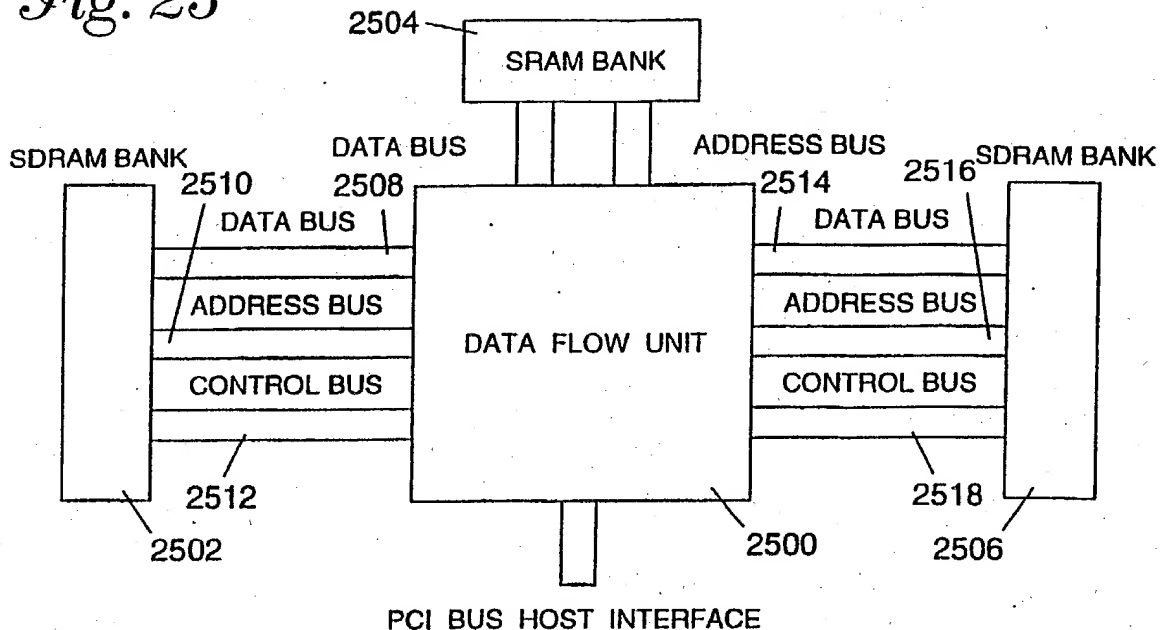


Fig. 24 BINARY OPERATOR WITH ONE EARLY OPERAND

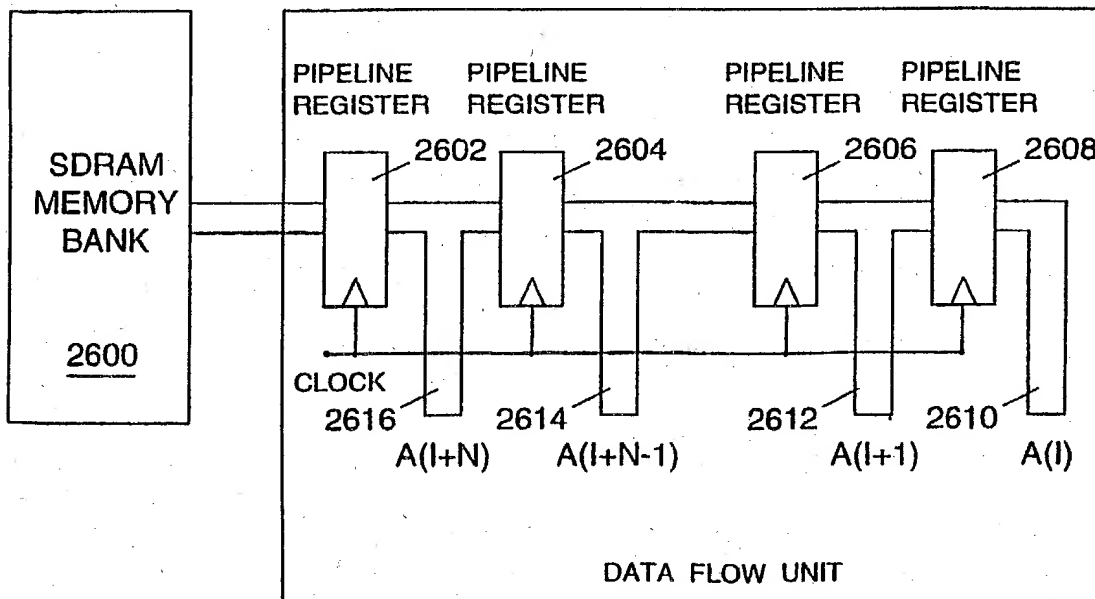
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Fig. 25



TYPICAL SYSTEM BLOCK DIAGRAM

Fig. 26

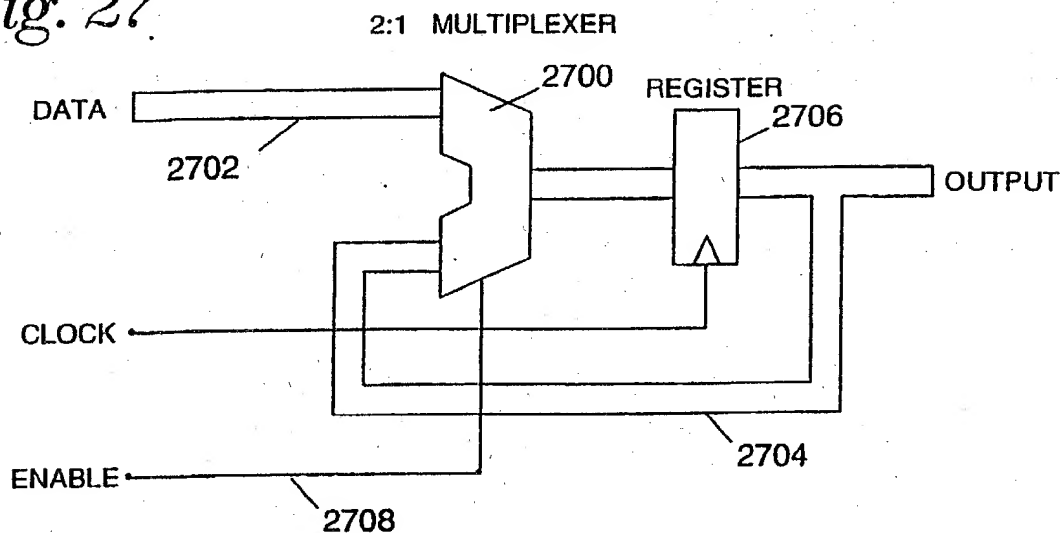


PIPELINING TO REDUCE MEMORY ACCESSES.



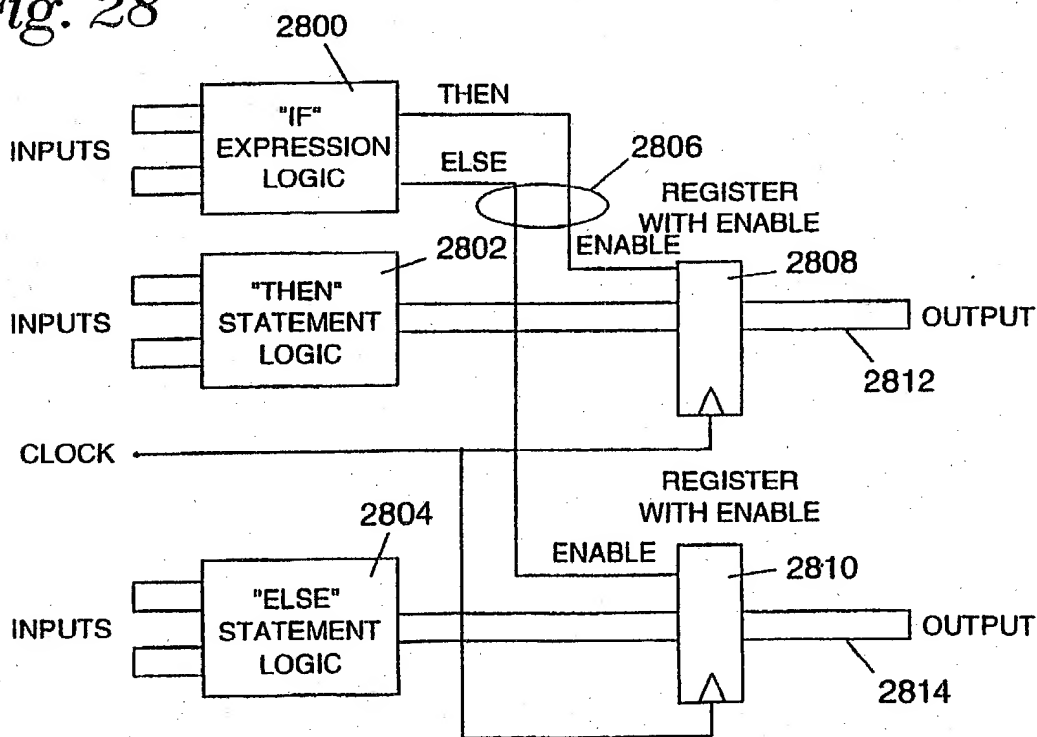
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Fig. 27



IMPLEMENTATION OF REGISTER WITH ENABLE

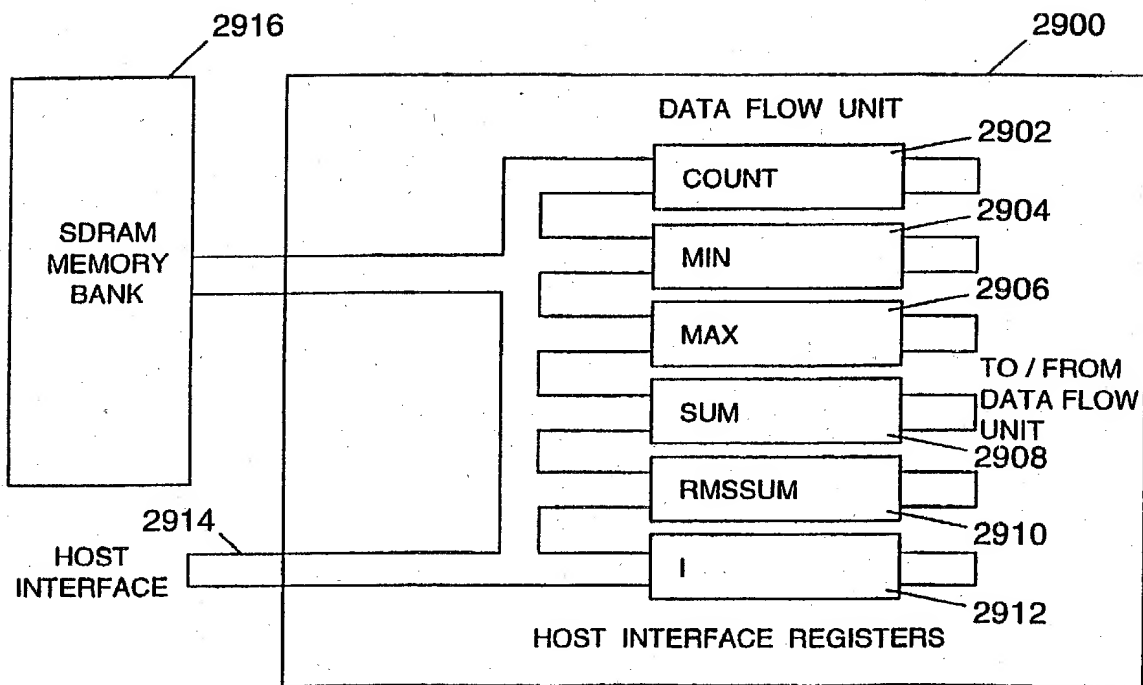
Fig. 28



HARDWARE IMPLEMENTATION OF CONDITIONAL STATEMENT.

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Fig. 29



EXAMPLE HOST INTERFACE/PROGRAMMING MODEL



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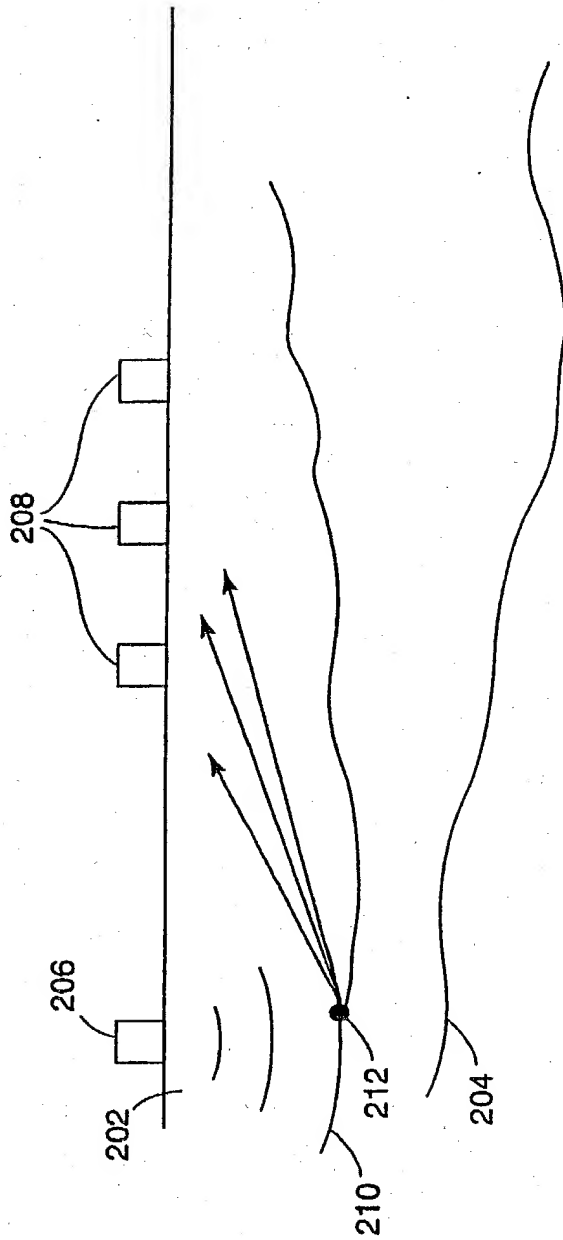


Fig. 30

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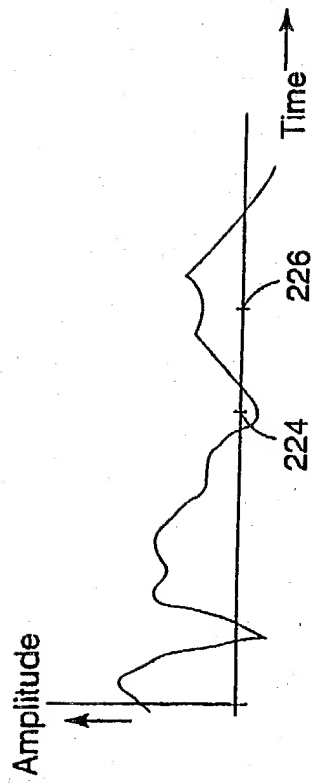


Fig. 31a

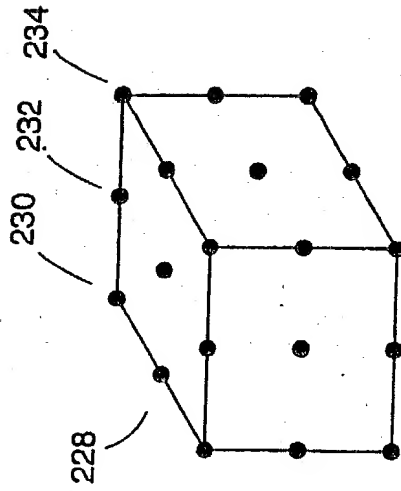


Fig. 31b

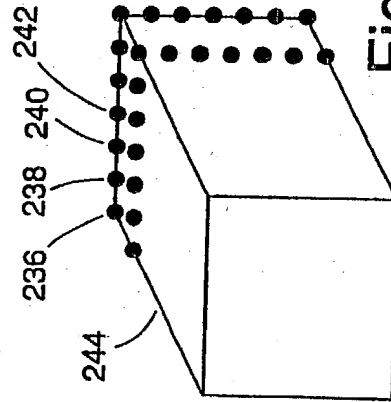
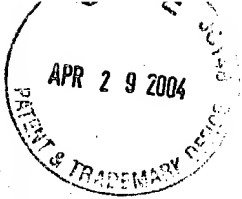


Fig. 31c



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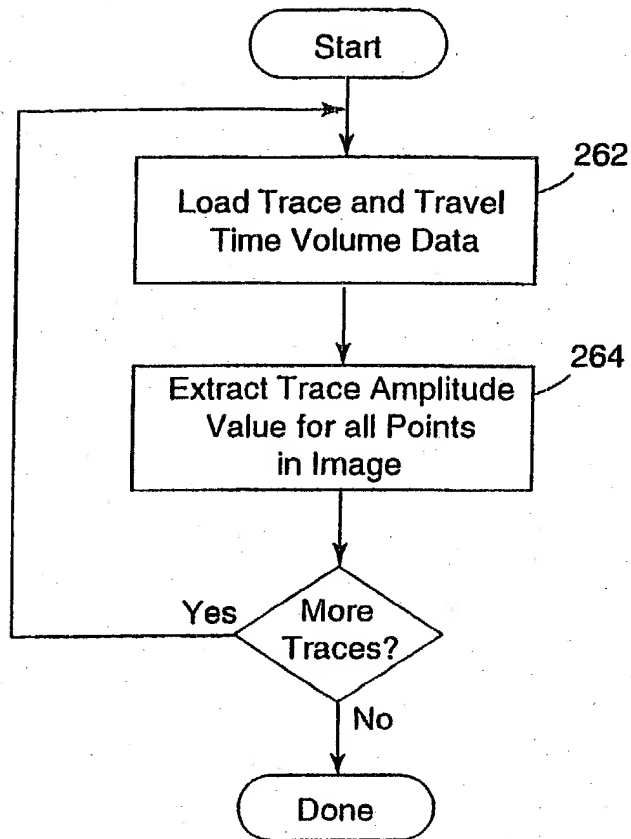


Fig. 32



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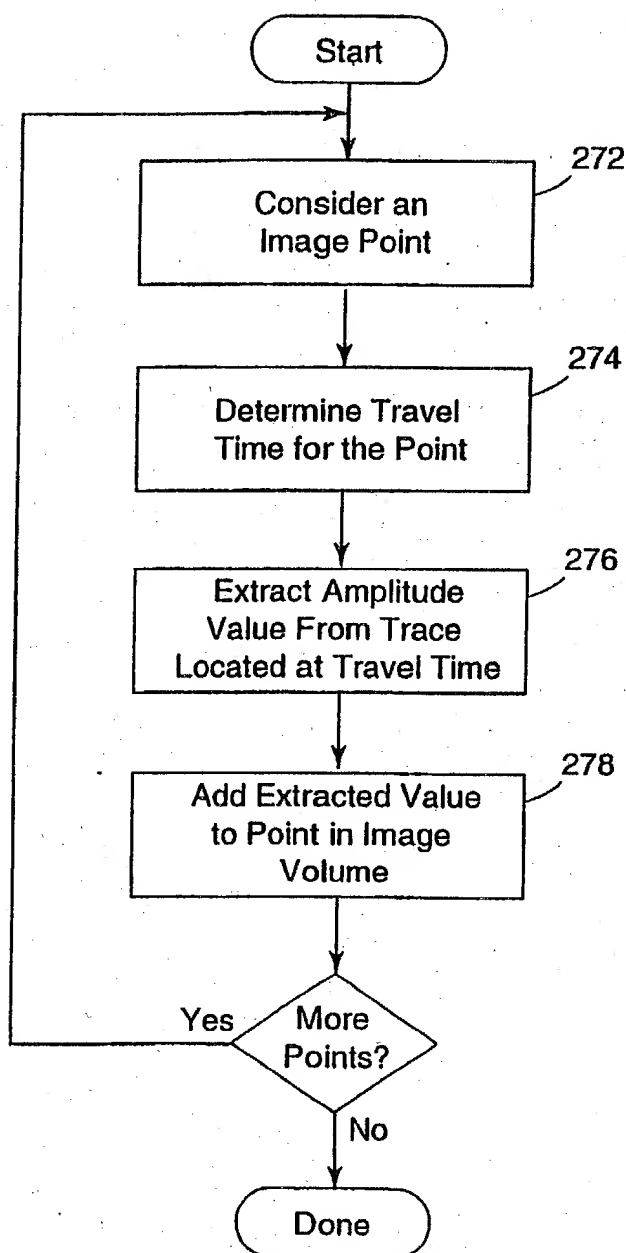


Fig. 33



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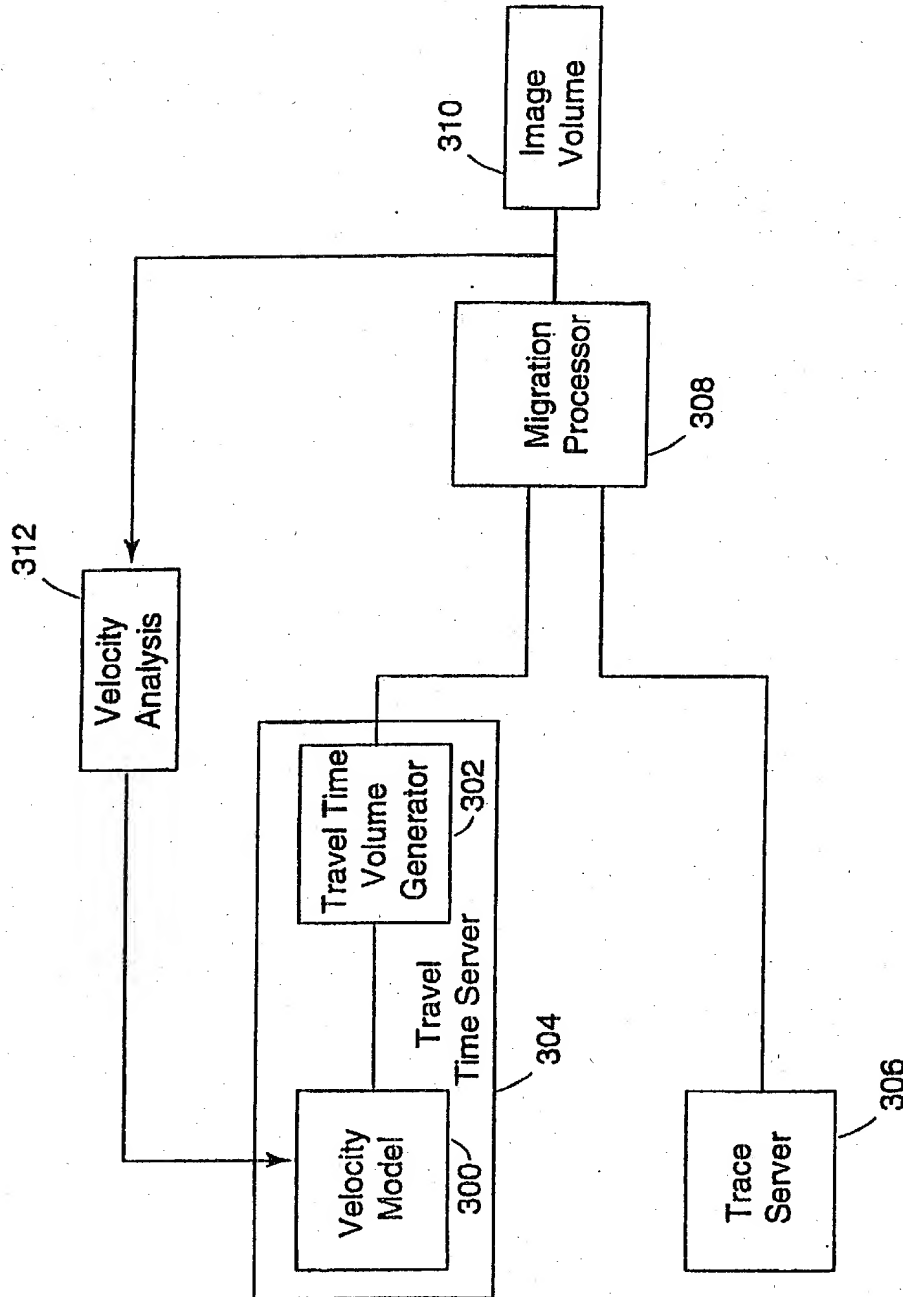


Fig. 34



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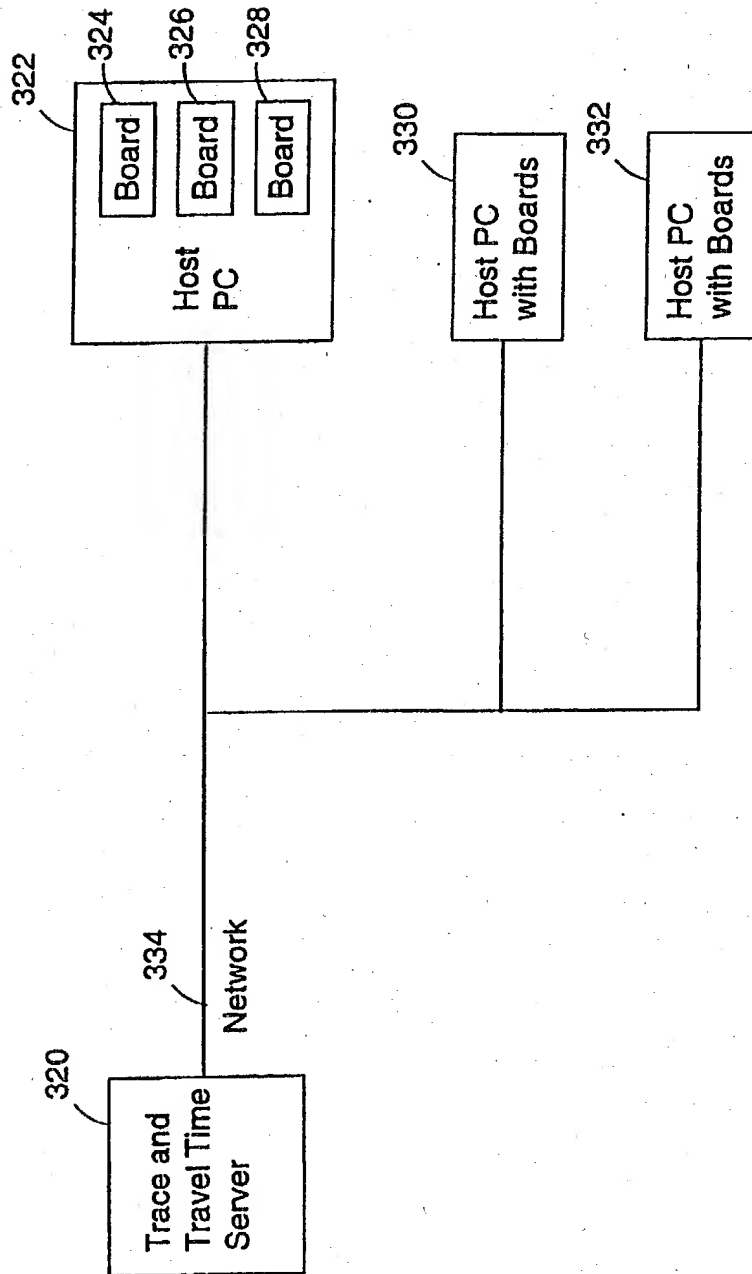


Fig. 35



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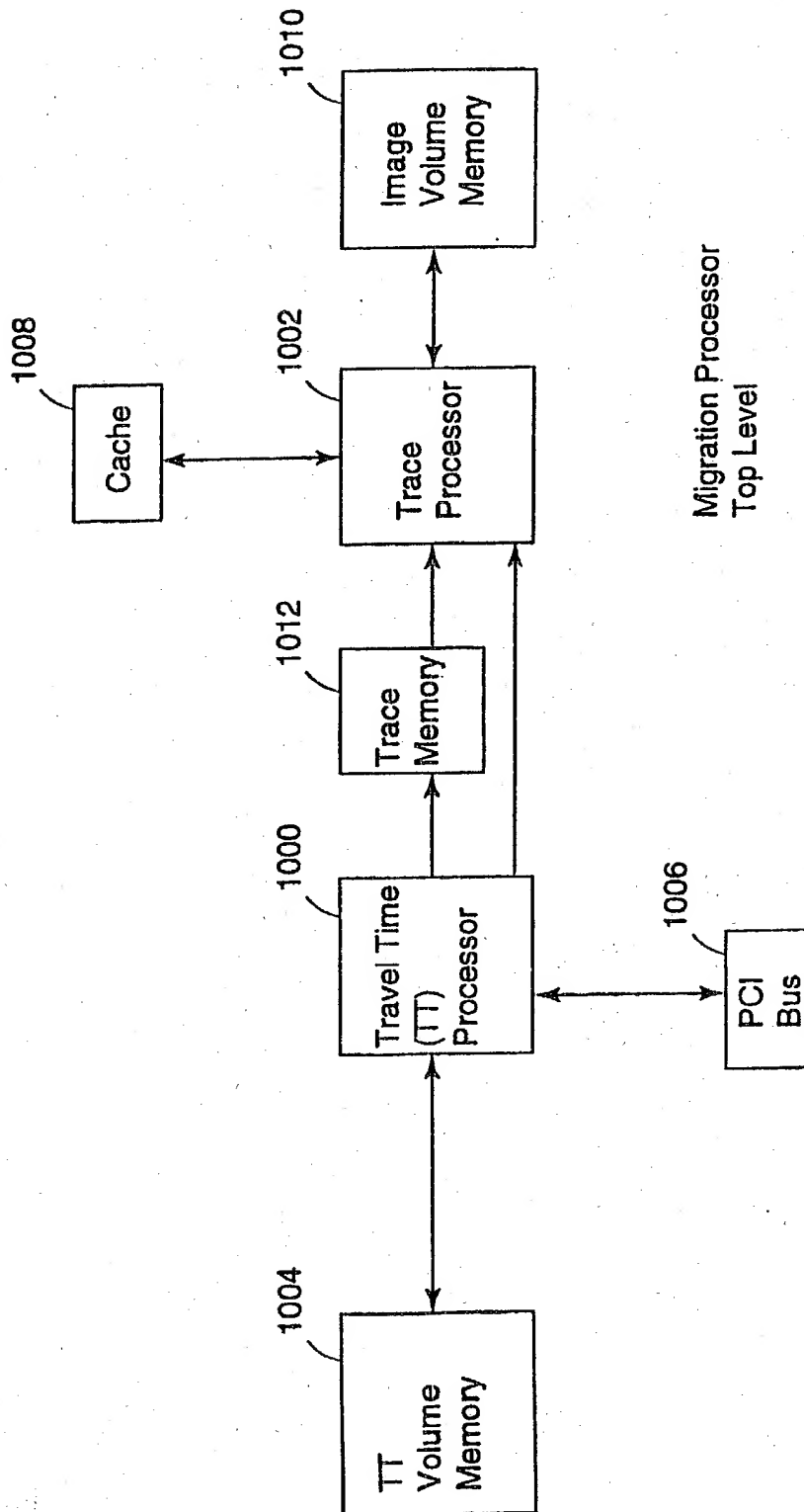
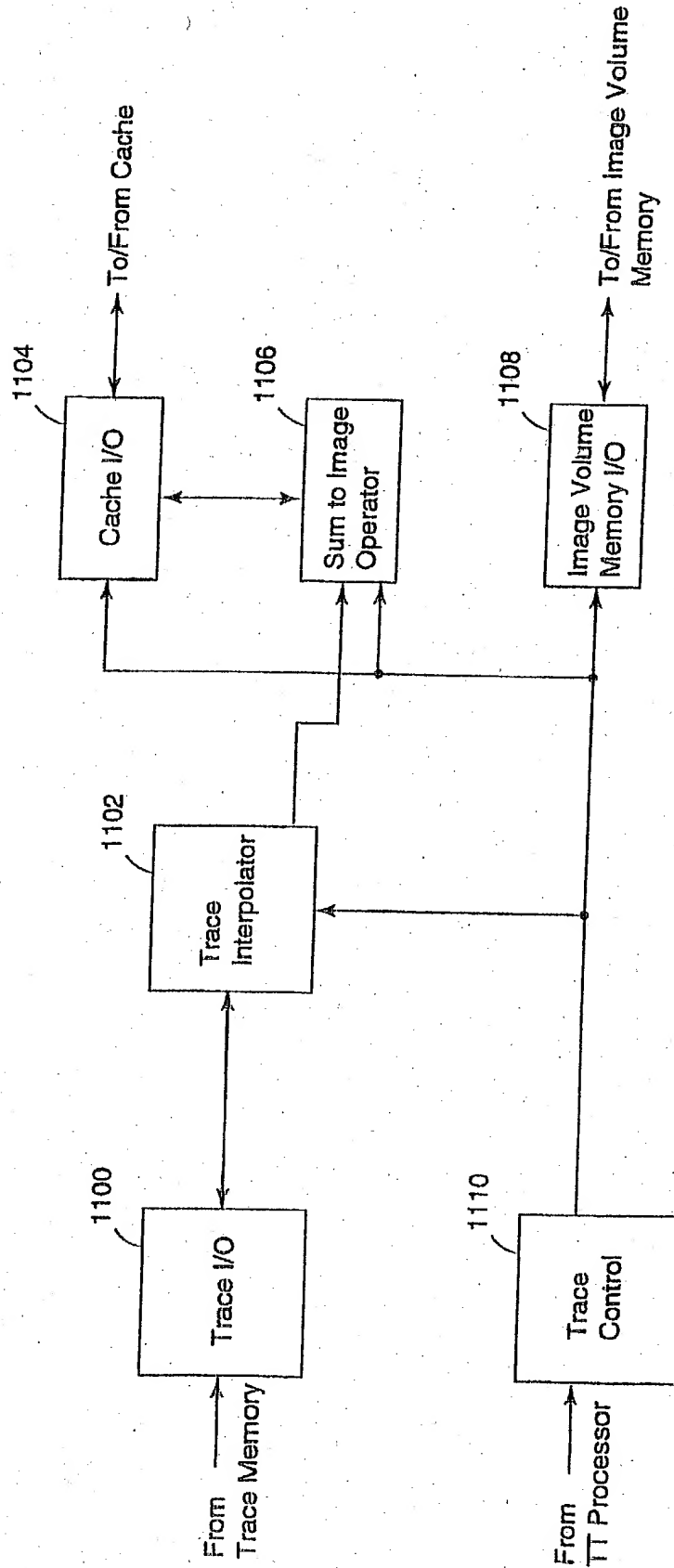


Fig. 36

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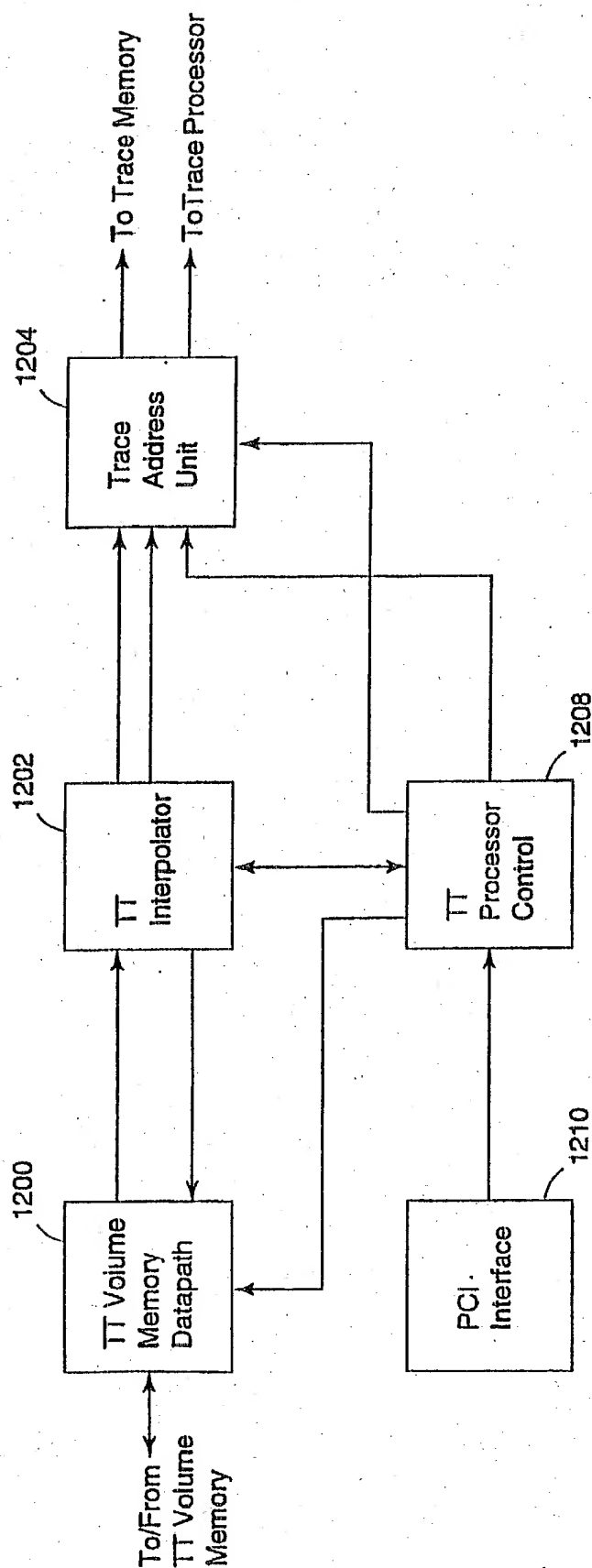


Trace Processor

Fig. 37



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Travel Time Processor

Fig. 38

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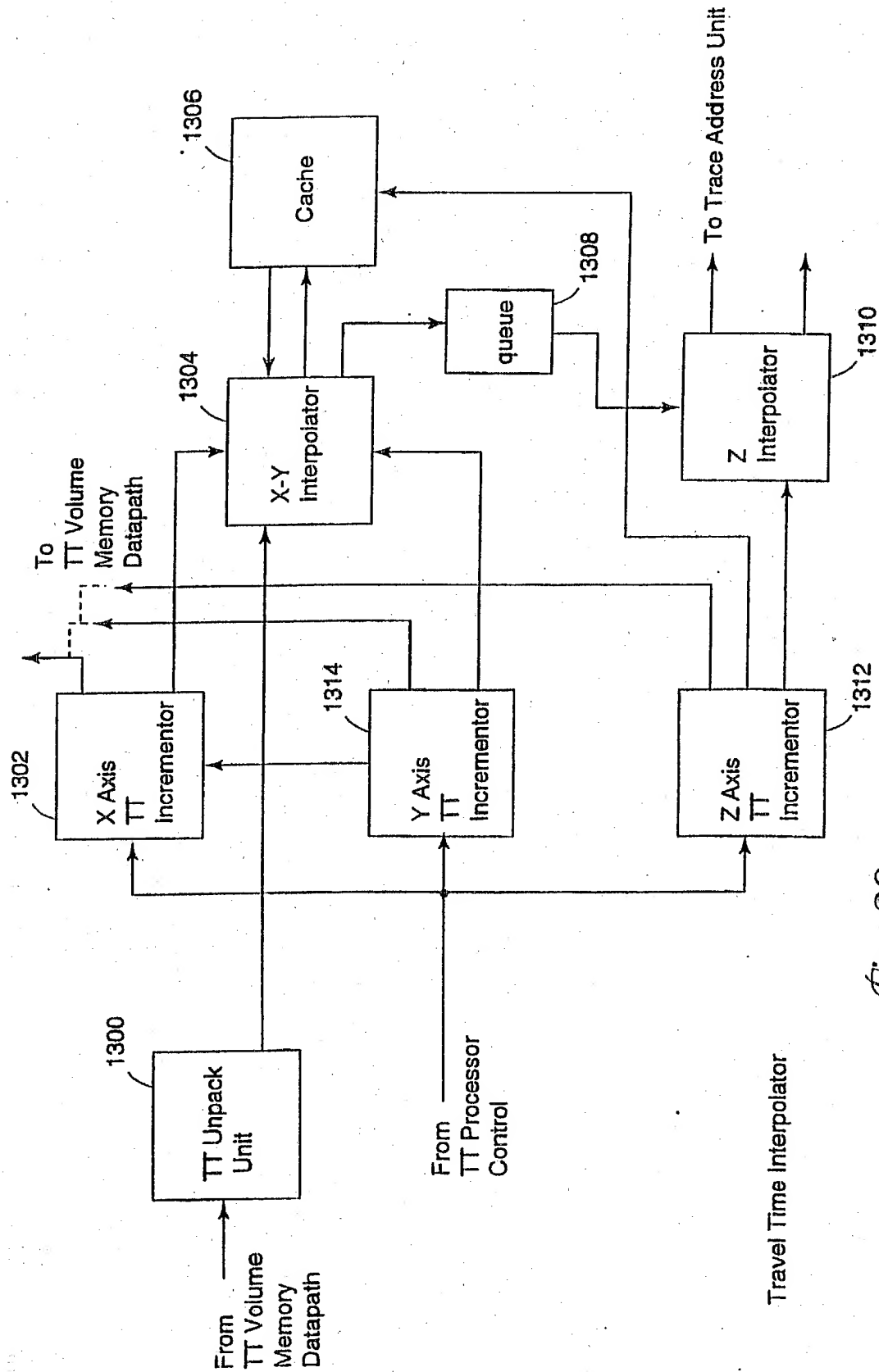


Fig. 39



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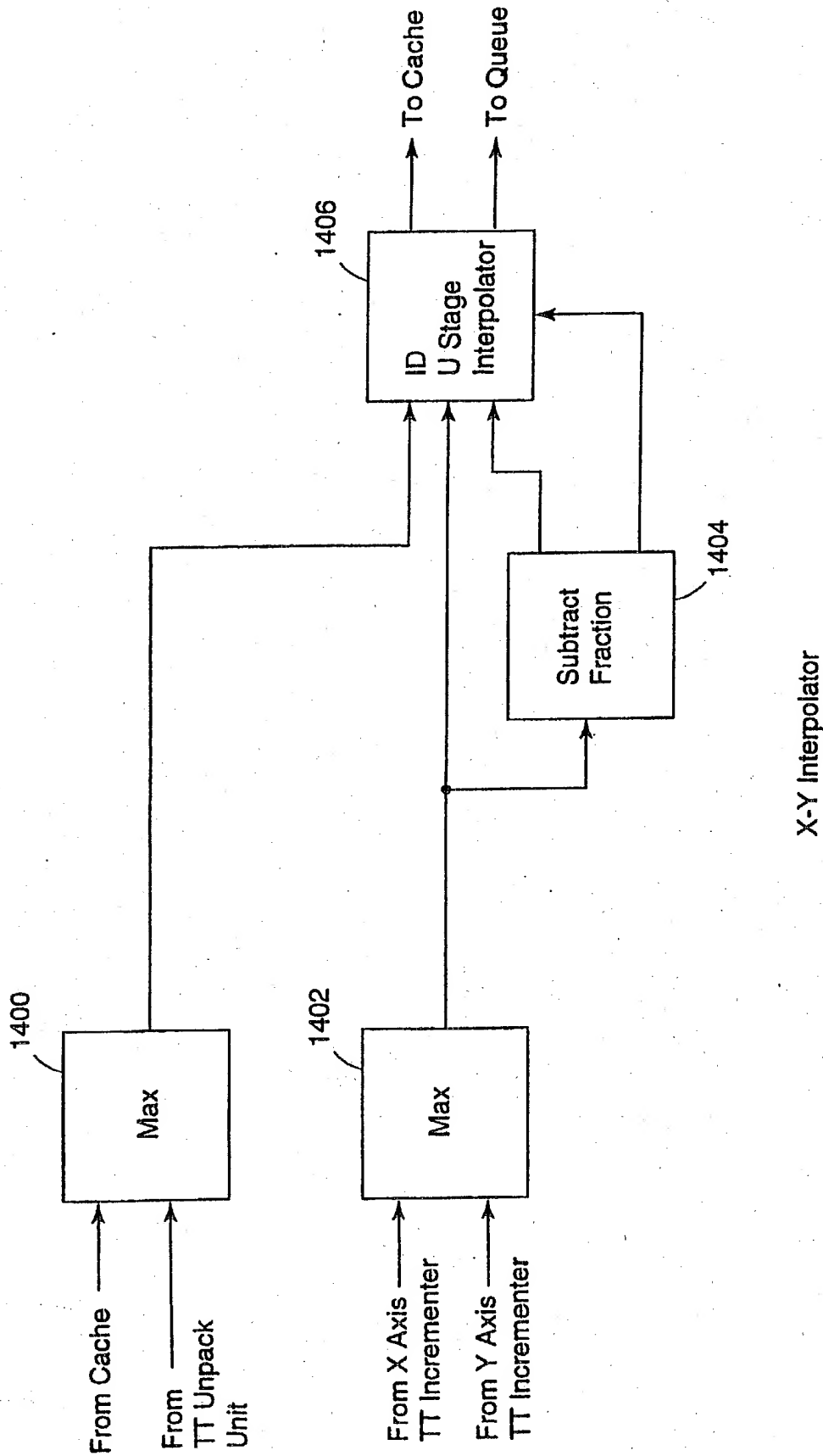


Fig. 40

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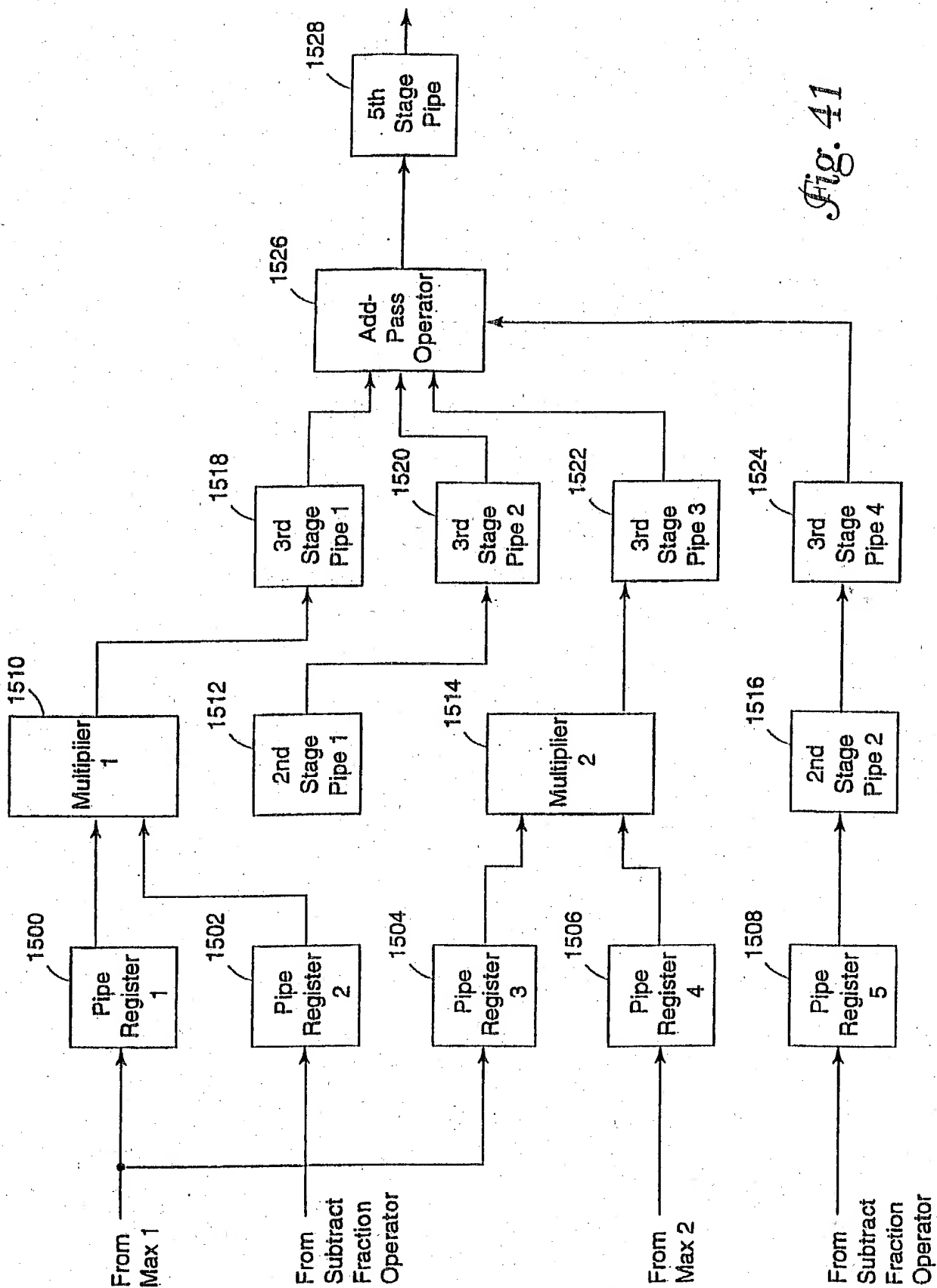


Fig. 41